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14. ABSTRACT

The growing need for large area display for home entertainment and the crossover to digital broadcasting has pushed the active matrix flat panel display industry to thrive over the past few years. The ability to make electronic devices that are transparent to visible and near infrared wavelengths with materials posing a high carrier mobility and high visual transparency is currently being researched. There has been a great interest in amorphous indium gallium zinc oxide (a-IGZO) as the active channel layer due to its promising electrical and photosensitive performance for thin film transistors with a high field effect mobility, low drain off current and good uniformity

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A Study of Electrical and Optical Stability of GSZO Thin Film Transistors

Briana S. McCall

North Carolina A&T State University

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Department: Electrical and Computer Engineering

Major: Electrical Engineering

Major Professor: Dr. Shanthi Iyer

Greensboro, North Carolina

2014

The Graduate School
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This is to certify that the Master's Thesis of

Briana S. McCall

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Dedication

This work is dedicated to God, through Him all things are possible, and to my family and friends for their support and encouragement.

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I would like to express my deepest gratitude to my major advisor, Dr. Shanthi Iyer, for her support and encouragement throughout my collegiate career here at North Carolina Agricultural and Technical State University. I would also like to thank Dr. Clinton B. Lee and Dr. Ward C. Collis for serving on my committee. Their guidance and insight were paramount in this research project and allowed me to learn more through its completion.

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Most importantly, I would like to thank my best friend Odavius Gilmore, for his unwavering love and encouragement of me as I pursued my degree. Without his constant love and support I would not have been able to complete this research project. The support of my family was very encouraging, as well.

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Table of Contents

List of Figures

List of Tables

List of Symbols

μ	Mobility
Au	Gold
CB	Conduction band
CBM	Conduction band minimum
C_{ox}	Oxide capacitance
Cu	Copper
D_{it}	Density of interface traps
DOS	Density of states
E_C	Conduction band energy
Ga	Gallium
GSZO	Gallium tin zinc oxide
GZO	Gallium zinc oxide
I_D	Drain current
IGZO	Indium gallium zinc oxide
In	Indium
I_{OFF}	Off current
$I_{ON/OFF}$	On/off current ratio
ITZO	Indium tin zinc oxide
IZO	Indium zinc oxide
M-OH	Metal hydroxides
N_2	Nitrogen gas
NBIS	Negative bias illumination stress
NBS	Negative bias stress
N_T	Total trap states
O	oxygen
O_2	Oxygen gas

PBIS	Positive bias illumination stress
PBS	Positive bias stress
q	charge
RF	Radio Frequency
RT	Room Temperature
SCCM	Standard cubic centimeter per minute
Si	Silicon
SiO_2	Silicon Dioxide
Sn	Tin
SS	Subthreshold swing
SZO	Tin zinc oxide
Ti	Titanium
TFT	Thin Film Transistor
UV	Ultra violet
V_G	Gate voltage
V_{DS}	Drain to source voltage
V_o	Oxygen vacancies
V_T	Threshold voltage
W/L	Width / Length ratio
XPS	X-ray Photoelectron Spectroscopy
Zn	Zinc
ZnO	Zinc oxide
ZTO	Zinc tin oxide

Abstract

The growing need for large area display for home entertainment and the crossover to digital broadcasting has pushed the active matrix flat panel display industry to thrive over the past few years. The ability to make electronic devices that are transparent to visible and near infrared wavelengths with materials posing a high carrier mobility and high visual transparency is currently being researched. There has been a great interest in amorphous indium gallium zinc oxide (a-IGZO) as the active channel layer due to its promising electrical and photosensitive performance for thin film transistors with a high field-effect mobility, low drain off current and good uniformity that is compatible with the state-of-the-art Gen-8 substrate size. However, as indium resources are becoming scarce and expensive, replacing the a-IGZO TFT with a less expensive material such as gallium tin zinc oxide (GSZO) has shown a potential to have similar electrical behavior. One of the issues of the oxide TFT, in general, is the optical and electrical instability. Hence, we have carried out a systematic and detailed study on the electrical and optical stability of these TFTs as a function of annealing temperature, deposition pressure, film thickness and oxide thickness to gain better insight into the degradation mechanism of these transistors as well as to correlate to the initial performance of the device. The analysis of stability measurements indicated that the post deposition annealing temperature of 350°C has the dominant effect on the reduction of the deep and shallow states, thereby making the device more stable. This also explains the superior performance of the initial device. The low temperature annealed device at 140°C appears to be influenced by the deposition pressure. Thus, this work shows that there is considerable room for improvement in both the TFT performance as well as its stability by tailoring the deposition parameters.

CHAPTER 1

Introduction

1.1 Overview

Despite the growing interest in the indium gallium zinc oxide (IGZO) display technology, IGZO uses rare-earth metals (indium and gallium), which introduces risk in procurement and cost increases. The applications of IGZO material enable higher resolution, lower power consumption, and higher performance on products ranging from liquid crystal display panels in mobile devices to large ultra-high definition flat-panel displays [1, 2]. As indium (In) resources are becoming scarce and expensive, replacing the *In* in IGZO TFTs with a less expensive and earth abundant material such as tin (Sn) having similar electronic configuration as *In*, has shown a potential to have similar electrical behavior. Bradley et al. [3]. have reported that amorphous gallium tin zinc oxide (GSZO) TFTs presented very good device performances after post annealing at 350˚C yielding the following characteristics: voltage threshold V_T -4 V, on/off current $1.4x10^6$, and subthreshold swing SS 2 V/decade. It was also reported that a-SGZO thin films prepared at room temperature by pulsed laser deposition and annealed at 500˚C, showed good performances, such as, a saturation mobility of ~2 $cm^2\ V^{-1}s^{-1}$, on/off current ratio of $\sim10^3$, and a V_T of 2.5 V [4]. It is important to note that the post deposition annealing temperature appears to play an important role in determining the characteristics of oxide semiconductors. Another important issue that all oxide semiconductors face is the degradation of the device performance with the illumination and under prolonged biasing [5]. GSZO material being a not so well studied alloy, many obstacles exist in the use of this material for practical device application because of the presence of traps in the channel, interface states, and the unknown valence configuration of *Sn*, which contribute to the degradation process of the device. Further,

the absorption and desorption of oxygen or H_2O from species on the ambient surface also leads to instability of the channel material, and hence impacts the TFT performance.

1.2 Research Objectives and Thesis Organization

Though there has been a strong interest in the IGZO TFTs, GSZO is still in the nascent stage. Like any new compound, the advancement and successful implementation of these devices would largely depend on the comprehensive understanding of GSZO material, device processing issues, and the degradation mechanism. In this thesis, we address the degradation mechanism. Hence the primary goal of this thesis is to provide a detailed assessment about the electrical and optical stability of GSZO TFTs under different deposition conditions as well as different post deposition annealing conditions.

The structure of the thesis is as follows. Chapter 2 gives a brief literature review of instability issues of TFTs. Description of oxide thin films devices performance due to stress is discussed to provide the background for the experimental work presented in this thesis. Chapter 3 provides a description of the characterization tools and techniques employed and a discussion of the electrical and optical characterization methodology. Chapter 4 describes the evaluation of GSZO TFT electrical and optical stability under different gate bias as a function of different bias periods. Finally, Chapter 5 concludes by providing a discussion of the results presented in the thesis and suggestions for future work.

CHAPTER 2

Literature Review

2.1 Introduction

There has been a great interest in adapting amorphous oxide semiconductors (AOS) to help them meet an adequate electrical performance. The positive attributes of the amorphous oxide TFTS are well known, such as high mobility, high transparency, low processing temperature, potentially good uniformity, and ease of fabrication [2, 6]. The high mobility in the amorphous phase has been attributed to the overlap of outer orbits of isotropic heavy metal ions that allows easy transport of electrons. Amongst the different oxide materials investigated, indium gallium zinc oxide (IGZO) TFTs have shown a promising electrical performance for TFT active layers with a high mobility (~12 cm^2/V-s), on/off current ratio (>10^7), small subthreshold swing (~0.1-0.4 V/decade), and expected good uniformity compatible with the state of the art Gen-8 substrate size [7, 8]. However, in our group, gallium tin zinc oxide (GSZO), an emerging material system, is shown to approach performance of IGZO devices [3, 5, 9, 10]. The stability of these transistors are one of the major concerns, and hence this thesis work is geared towards the stability of GSZO TFTs, which were annealed at higher temperature with superior performance as well as annealed at lower temperature for flexible electronics applications. This chapter introduces an overview of the research carried out on IGZO, ZnO, and GSZO thin film transistors that is relevant to the work discussed in this thesis.

2.2 Surface Roughness and Microstructure of Oxide Thin Films Transistors

The impact of interface microstructure has a significant effect on the device performance. Device characteristics such as channel mobility were found to be improved with the interface smoothness [11]. Since thin film device performance is highly dependent on the density of

surface states and its morphology, a highly smooth surface is desirable because it has no surface induced effects as compared to the case of highly rough surfaces [12].

2.3 Charging and Trapping Dynamics in Oxide TFTs

There are two possible mechanisms responsible for device degradation, which could be due to trapping of charges in the channel/interface or the creation of defect states in the deep gap states of the channel interface [13]. Nomura et al. [14], examined the origins of voltage threshold shifts by studying the stress dynamics in a-IGZO TFTs deposited at room temperature, and annealed at 400°C in dry or wet O_2 atmospheres. Stress and recovery data was found to be well fit by the following stretched exponential function:

$$\Delta V_{th} = \Delta V_{th0}\left[1 - (\exp(-(t/\tau)^{\beta}\right] \qquad (2.1)$$

where ΔV_{th0} is the ΔV_{th} at infinite time, β is the stretched-exponential exponent, and τ is the trapping time for the stress phase and detrapping time for recovery phase. This work yielded τ and β values to be 5.8 x 10^4 s and 0.57 for the unannealed, 4.1 x 10^4 s and 0.64 for the dry annealed, and 1.8 x 10^4 s and 0.70 for the wet annealed a-IGZO TFTs, respectively. Similar results were reported in a study by Lee et al. [15] of an annealed a-IGZO with τ = 2 x 10^4 s and β = 0.42.

Chen et al. [16] investigated the origin of the bias stress effect in oxygen adsorption zinc tin oxide TFTs by studying the dynamics of the stressing process in different ambient oxygen partial pressures for 1000 s. For stress, the threshold voltages (V_T) of the ZTO TFTs were defined as the gate voltage where the drain current reaches 10 pA. Figure 1. shows the average time when oxygen adsorption (trapping) and desorption (detrapping) occur. Observed trends as the pressure increased: 1) ΔV_T increase, 2) trapping time decrease, 3) detrapping time increased. Previous studies suggested that the oxygen molecules can capture electrons from the conduction

band and then adsorb on the device as a form of $O_2 + e^- \rightarrow O_{2(ads)}^-$, causing a depletion layer in the active backchannel and an increase in the ΔV_T of ZTO TFTs [17, 18].

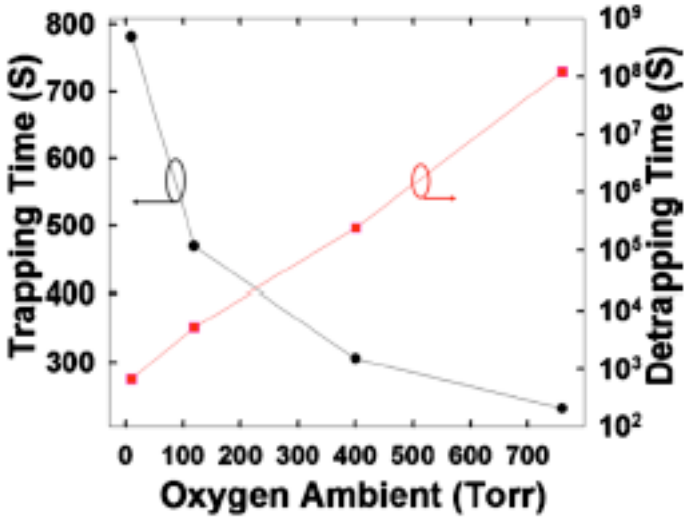

Figure 1. Characteristic time constant for oxygen adsorption and desorption for different ambient oxygen pressure.

Nguyen et al. [19] investigated the influence of thermal treatment on the stability of ITZO TFTs for 10^4 s. Observed trends as the annealing temperature increased: 1) the number of shallow traps decreased, 2) the device improved, 3) ΔV_T decreased, and 4) trapping time which the electrons were trapped also decreased, as shown in Figure 2. Kamiya et al. [20] stated that thermal annealing remove weak chemical bonds, such as Zn-O and form a stable a-IGZO.

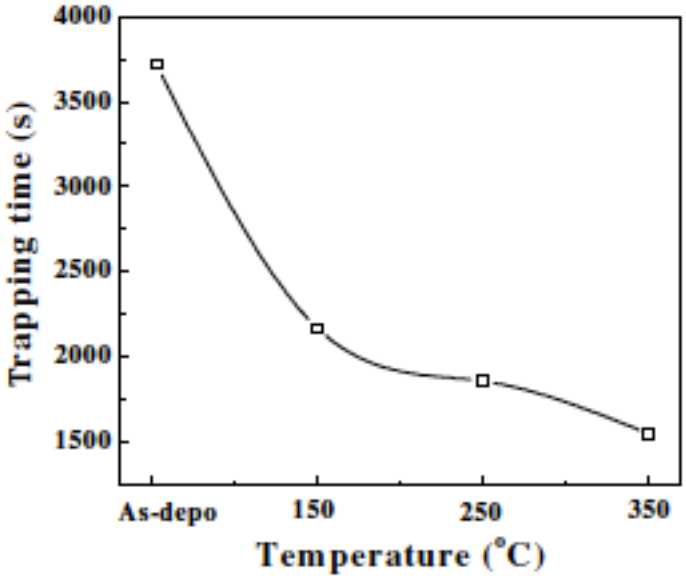

Figure 2. Trapping time characteristics of carriers of devices with different annealing temperature under bias stress.

Yun et al. [21] investigated the instability of ZTO TFTS with different channel thicknesses t_{ch}. Observed trends as the t_{ch} increased: 1) ΔV_T decreased, 2) the instability under the positive bias stress was improved, and 3) τ increased. Figure 3. shows the behavior of τ with increasing t_{ch}, which was similar to the behavior of τ with decreasing oxygen partial pressure reported by Chen et al. [16].

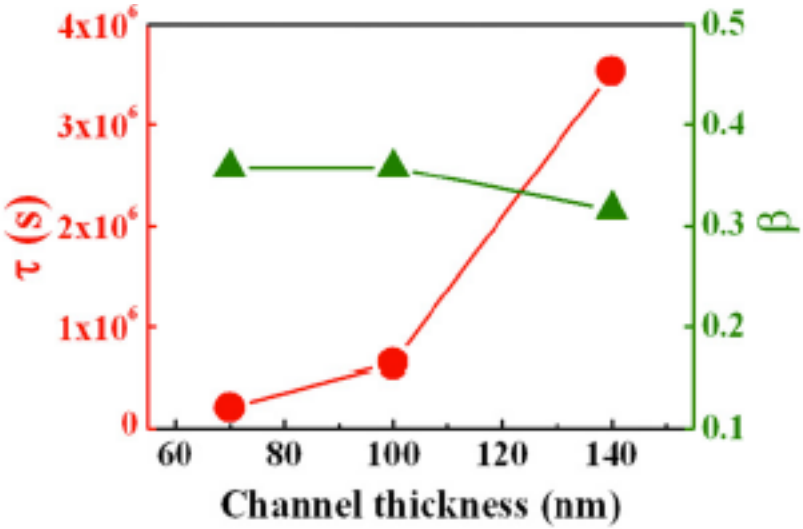

Figure 3. Extracted fitting parameters of ZTO TFTs with different channel thicknesses.

This behavior indicated that the reduction of the ambient oxygen effect is due to the less gate field, meaning that the thickness dependence of τ implies the reduced effect of the ambient oxygen on the positive bias-induced instability with increasing t_{ch}.

The trapping time constant τ represents the time it takes a carrier to trap itself inside the insulator. The degree of diversion from the exponential function is described by the stretching parameter β, which is limited ($0< \beta \leq 1$). A stretching parameter close to 1 indicates a narrow distribution of time constants, while a smaller stretching parameter ($\beta <1$) implies a broader distribution of time constants [22].

It has been proven that linear dependence of β is different between the annealed and unannealed IGZO TFTs: 1) a linear dependence of β originates from multiple trapping states and 2) a temperature independent of β is due to tunneling or hopping mechanism [23]. According to Nomura et al. [14], this indicates that thermal annealing alters the dominant mechanism for the V_{th} shift and its origin is in the channel insulator interface.

A comparison of dynamic positive bias stress parameters for oxide TFTs extracted in published work is presented in Table 1. The fitting parameter τ and β typically range at 10^2-10^6 s and 0.3-0.6, respectively. These studies revealed that positive bias instability was due to oxygen molecules capturing electrons from the conduction band then adsorbing on the devices and weak chemical bonding of Zn-O. However, the reduction of ambient oxygen effect is due to less gate field and the removal of weak chemical bonds is due to thermal annealing. Hence, form a more stable device. Dao et al. [24] concluded that the further annealing leads to decreases in carrier trapping time.

Table 1

Comparison of stress parameters for oxide TFTs extracted in published work

Material	Condition	Stress/ Recovery	τ (s)	β
ZTO Ref. [21]	70 nm 350°C 3 hr	Stress	2.1×10^5	~0.35
	100 nm 350°C 3 hr		6.4×10^5	~0.35
	140 nm 350°C 3 hr		3.5×10^6	~0.3
a-ITZO Ref. [19]	As-deposited	Stress	3.72×10^3	-
	150°C 1 hr		2.17×10^3	-
	250°C 1 hr		1.86×10^3	-
	350°C 1 hr		1.55×10^3	-
a-IGZO Ref. [25]	1% H_2+99% N_2 1hr	Stress	5.0×10^3	0.42
	O_2 1 hr		1.5×10^4	0.42
	Air 1 hr		2.0×10^4	0.42
	Vacuum 1 hr		6.3×10^4	0.42
ZTO Ref. [16]	350°C 1 hr 10 Torr	Stress	~8.0×10^2	-
		Recovery	~3.0×10^2	-
	350°C 1 hr 120 Torr	Stress	~4.8×10^2	-
		Recovery	~3.5×10^2	-
	350°C 1 hr 400 Torr	Stress	~3.0×10^2	-
		Recovery	~5.0×10^2	-
	350°C 1 hr 760 Torr	Stress	~1.0×10^2	-
		Recovery	~7.0×10^2	-
a-IGZO Ref. [14]	Unannealed	Stress	5.8×10^4	0.57
	400°C 1 hr Dry annealed		4.1×10^4	0.64
	400°C 1 hr wet annealed		1.8×10^4	0.7
a-IGZO Ref. [15]	300°C 30 mins 5 mTorr	Stress	2.0×10^4	0.42

2.4 Electrical Stability of AOS TFTs

To further investigate the trapping dynamics, stress measurements were performed with various deposition parameters. Dao et al. [24] reported that the shift in the positive direction under positive bias stress was due to the generation of defects originating from the creation of

dangling bonds or electron trapping near the gate insulator interface in IGZO thin film transistors.

Mathews et al. [13] indicated that subjecting TFTs to a prolonged bias stress can alter its electrical parameters due to device degradation, as shown in Figure 4. In this case, a positive and negative gate bias stress of 20 V was applied for time periods ranging from 10 s to 10^5 s. A positive shift in the transfer characteristics and variation of drain current with gate voltage followed a similar pattern over different stress times. This provided evident that no additional defect states were created and the positive shift in threshold voltage was a direct result of trapping of electrons at the channel/dielectric interface [26].

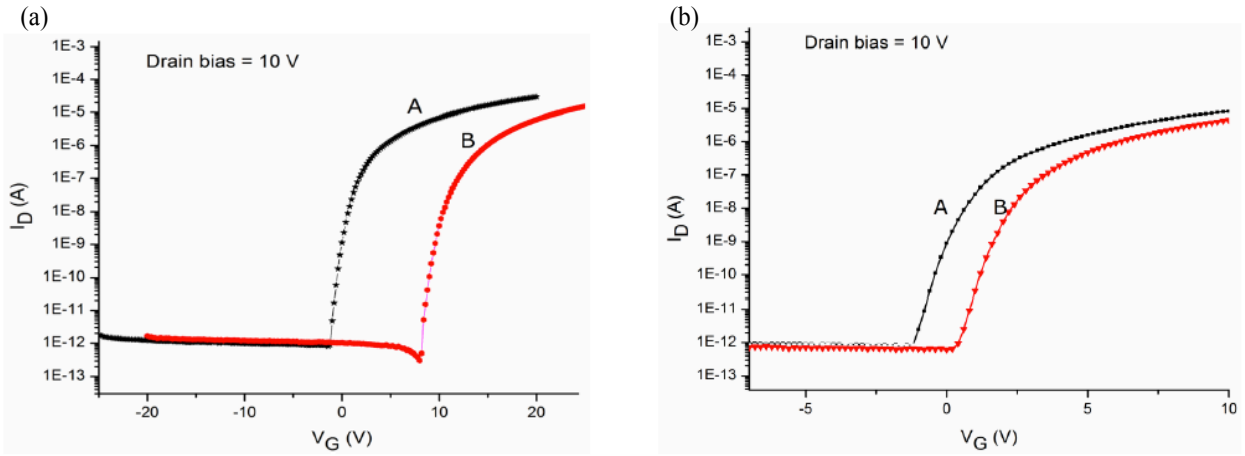

Figure 4. Transfer characteristics at V_{DS} = 10 V of IGZO TFT after (a) positive gate bias stress and (b) negative gate bias stress with V_G = 20 V for 10^5 s.

Jeon et al. [27] reported that the movement of hydroxyl groups cause the instability of the ZnO TFT under both positive and negative bias stress of 20 V. This research group focused on the different gate insulator material (such as Type I SiO_2, Type II Al_2O_3, Type III Al_2O_3) and deposition temperature (100-200 C) of the ZnO layer. Major findings included: a) the instability of the ZnO TFT under positive gate bias decreases with increasing deposition temperature at the active layer, b) the instability under negative gate bias stress is related to the gate insulator

material or to the insulator deposition process. From this study it was concluded that increasing the deposition temperature reduces the number of hydroxyl groups and improves the electrical characteristics of ZnO TFT. Many studies have reported the degradation mechanism of both positive and negative bias stress on AOS TFTs. Table 2. summarizes all possible causes for the observation that were made at each stress condition.

Table 2

Degradation mechanism of the application of PBS and NBS.

Application	Observation	Cause
PBS	Positive shift	Electron trapping at the gate insulator and/or interface [28]
		Creation of trap states in the active channel [29].
		Creation of acceptor-type deep traps-unoccupied defects that can accept extra electrons [15, 23]
	Negative shift	H^+ or OH^- species become incorporated into the channel during deposition [30].
		Excess holes get injected from the gate electrode into interface, damaged during the sputtering process [30].
NBS	Positive shift	Trapping of electrons at the channel/dielectric interface [13]
		Dominated by the variation of oxygen vacancies at or near the channel/insulator interface [31].
	Very minimal negative shift	Hole trapping is negligible [31].
		Electrons accumulating on the channel are being trapped in the intermetal dielectric layer [29].
		Charge trapping rather than the creation of defects [32]
		The Fermi level E_F can hardly be lowered toward E_V for hole accumulation; therefore it is negligible [33].

2.5 Optical Stability of AOS TFTs

2.5.1 Optical properties of thin films. It was reported that the photosensitive behavior of a-IGZO TFTs depends on the absorption. The absorption coefficient is related to the concentration of free electrons by:

$$a = \frac{N_e q^2 \lambda^2}{8\pi\varepsilon_0 n\tau m^* c^3} \qquad (2.2)$$

where a= absorption coefficient, N_e= concentration of free electrons, q= electron charge, λ= absorption wavelength, ε_0=dielectric constant in vacuum, n=refractive index, τ=relax time, m^*=effective mass of free electrons, and c=optical velocity. Optical transmission spectra of thin films can provide the absorption coefficient, α, using the following equation:

$$\alpha = \left(\frac{1}{d}\right) \ln\left(\frac{1}{x}\right) \qquad (2.3)$$

where d is the thickness of the thin film and x is the absorbance [34]. Using the Tauc relation, the optical band gap can be estimated from absorption coefficient data as a function of wavelength:

$$\alpha h\nu = B\left(h\nu - E_g^{opt}\right)^n \qquad (2.4)$$

where $h\nu$ is the photon energy, E_g^{opt} is the optical band gap, B is band tailing parameter and n = ½ for direct band gap and n = 2 for indirect band gap [35]. However, the E_g^{opt} of a thin film can be determined by extrapolation of the best line of fit from the graph of $(\alpha h\nu)^{1/2}$ vs $h\nu$ as shown in Figure 5. [36]

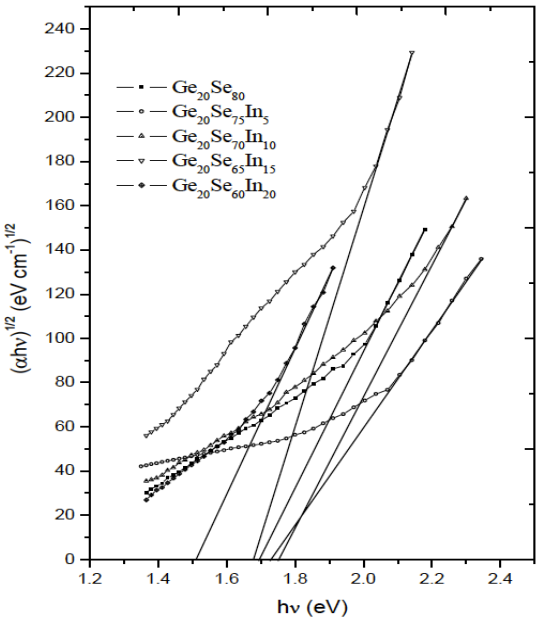

Figure 5. Tauc Plot of $(\alpha h\nu)^{1/2}$ vs $h\nu$ for GeSeIn thin films

Yao et al. [18] calculated the optical bandgap of a-IGZO of different oxygen content to be 2.6, 2.8, and 2.9 eV using the Tauc plot, indicating band-gap widening effect for the film with a low electron density. These results showed that photons with energy higher than 2.6 eV exhibited the photoelectric effect, as shown in Figure 6. It was reported that oxygen content of the channel layer has significant effects on the electrical and photosensitivity characteristics of IGZO TFTs.

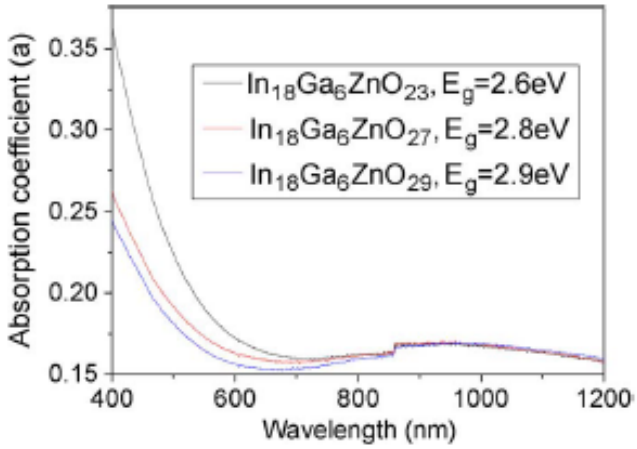

Figure 6. Absorption spectra of a-IGZO films.

There are different energy levels within the semiconductor optical band gap, such as deep and shallow states as shown in Figure 7. Deep states are associated with defects or impurities in the middle of the band gap; shallow states can trap the excited electrons near the conduction band or valence band. When the incident radiation has energy higher than the band gap, the photons can be absorbed by the semiconductor, transferring their energy to an electron [37].

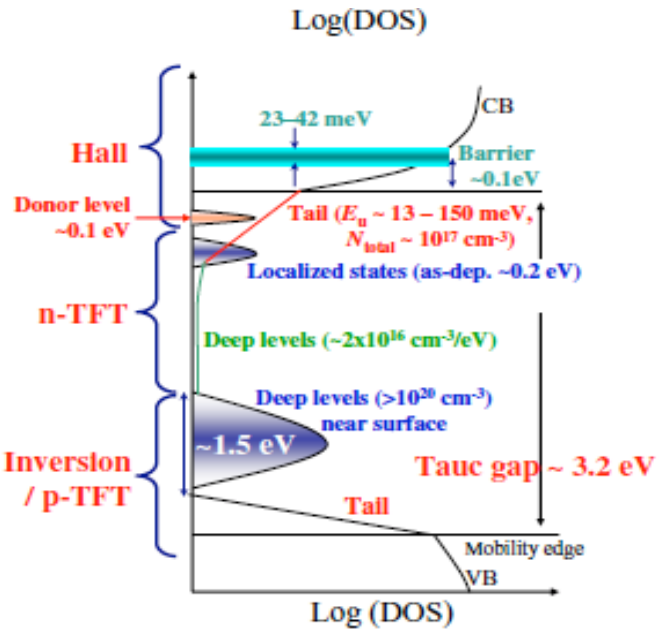

Figure 7. Schematic model of subgap DOS in a-IGZO.

2.5.2 Photo-instability. To understand the effect of prolonged exposure to light illumination, stress test were done by exposing TFTs to continuously wide wavelengths of lights to excite trapped carriers, which provided an understanding of the energy distribution and density of traps within the structure [38]. Figure 8. shows the typical response to monochromatic light of transfer characteristics of passivated a-IGZO TFTs as a function of wavelength and photon energy. The blue lines correspond to illumination above the band gap and the black lines correspond to subgap illumination.

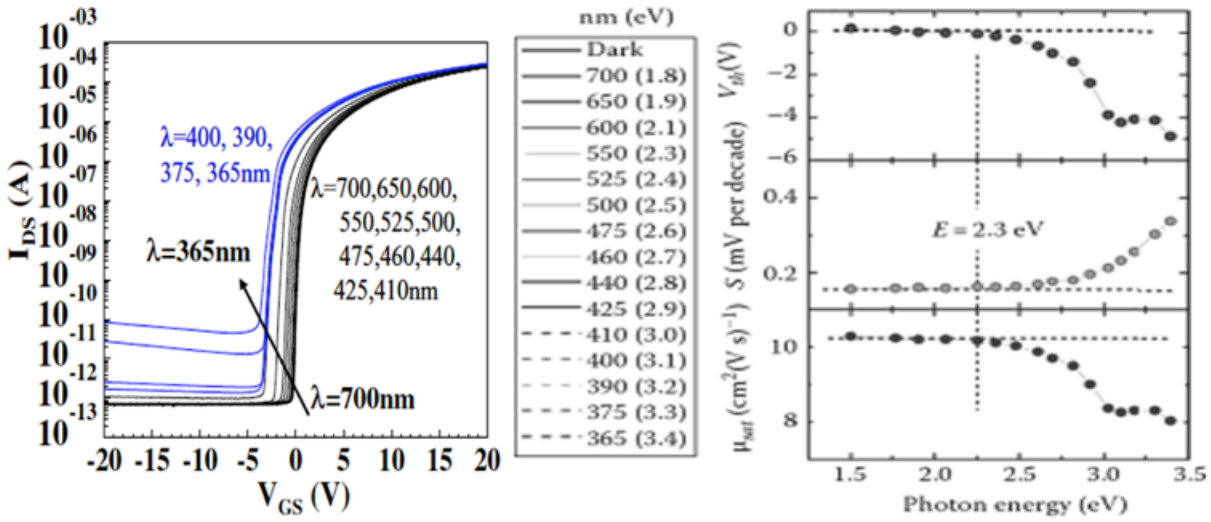

Figure 8. Typical photoresponses of a-IGZO TFT as a function of photon energy.

As observed, a-IGZO TFTs respond to photon energies above 2.3 eV, which is lower than the band gap (3.1 eV). At these photon energies, the off current and subthreshold swing increases, and the V_{th} and mobility decrease. This is attributed to excitation of electrons from the deep subgap states to the conduction band [20]. However, when a negative bias is applied in combination with the illumination stress, a large deviation of V_{th} is observed, as shown in Figure 9c.

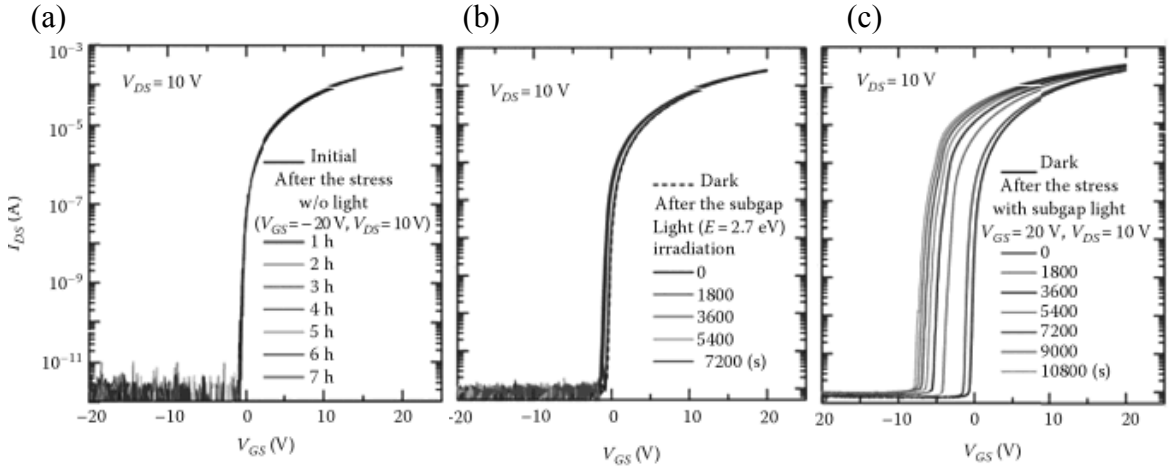

Figure 9. Typical stability of a-IGZO TFT under (a) negative bias only, (b) subgap light illumination only, and (c) NBIS.

This indicated the valence band maxima defects at 2.3 eV below the conduction band maxima was eliminated by subgap photons excitation up to 2.9 eV [39]. This also indicated that the negative bias illumination stress (NBIS) is due to the following: 1) generation of electron-hole pair at the back channel surface near-VBM states, 2) diffusion of holes or other positive charges like H^+ to the depletion layer, and 3) hole/positive charge trapping by defects at the gate/insulator/channel interface. A schematic illustration of this process is shown in the Figure 10.

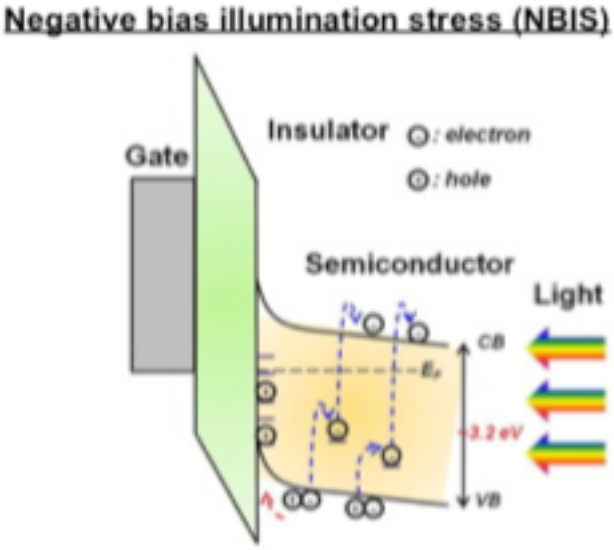

Figure 10. Schematic of a-IGZO under NBIS instability.

A summary of the degradation mechanism of photo-instability induced on oxide TFTs has been summarized in Table 3.

Table 3

Degradation mechanism of an application of Illumination Stress, NBIS, and PBIS

Application	Observation	Cause
Photon energies below 2.3 eV	Small Negative Parallel shift of V_{th}	All the subgap states are fully occupied below the Fermi level
Photon energies above 2.3 eV	Large Negative Parallel shift of V_{th} Increases in D_{it} near CB	Excitation of electrons from deep subgap states to the conduction band [20] [29].

Table 3

Cont.

		Generation of doubly ionized oxygen vacancies (V_O^{+2}) [29, 40].
		the photo-desorption of the adsorbed oxygen ions onto the channel surface [41].
Photon energies above optical bandgap (3 eV)	Degradation of V_{th} and SS	Photo-induced carriers [42].
NBIS	Negative shifts of transfer curve V_{th} decrease with increasing photon energy	Hole trapping at the channel/insulator interface or insulator [40].
		Accumulation of ionized oxygen vacancies (V_O^{+2}) at the interface [40].
		Transition from Vo to Vo^{+2} states; photogenerated holes rather than defect state creation [28]
PBIS	Repels photo-generated holes away from the gate insulator	Negligible hole trapping [28]

Various studies have shown that the wavelength greater than 500 shows little to no change whereas smaller wavelengths significantly affect the response of the TFT transfer characteristics [29, 33, 40, 43]. Mobility is not affected by the photo-illumination stress, which indicates a strong UV photon absorption in the channel layer and the electron-hole pairs generated contributes directly to the conductivity, leading to large negative V_{ON} shift [43].

Under a positive gate bias the Fermi level E_F is close to conduction band, therefore light illumination would caused electron generation from local states to conduction band, thus increasing the electron density at the channel layer. For oxide-based material n-type semiconductors it is apparent that the generated electrons by light illumination is negligible compared to active layer electron density under positive gate bias. This is one of the reasons why the effect of light under positive gate bias stress has been ignored [44]. The absorption of light with smaller photon energy than the E_{opt} could occur through localized states, thus generating

hole carriers from localized state to valence band. Oh et al. investigated other origins of degradation of NBIS and revealed that ionized oxygen vacancy sites (V_O^{2+}) act as deep hole traps and provide free electrons carriers in, which in turn result in negative shift in V_{th}.

Highlights of this study include but are not limited to: a) there is little to no shift in transfer characteristics at higher wavelengths greater than 500 nm, b) as the wavelength of light used is reduced, the turn-on voltage gets smaller, c) photon energies above a TFT bandgap can lead to band-to-band transition of carriers from the valence band to the conduction band, d) as gate increases, Fermi level moves toward conduction band and the electrons fill up the energy state and trap site beneath the E_F in the bulk of the active layer and at the interface e) mobility barely changed under any wavelength light [29, 42].

2.6 Modeling of Oxide TFTs

To understand the device physics and the TFT operation, a parameter extractor is essential. There are a few reports on modeling the current-voltage characteristics of oxide TFTs. Hossain et al. have developed a numerical model and simulation based on grain-boundaries in ZnO TFTs using a device simulator to calculated the approximate range of trap states densities localized in GBs. However, there is a AIM-SPICE Si:H Level 15 model that uses exponential distributions of deep and tail states, and has been used for IGZO TFTs [45]. This method is only useful for linear and saturation regions for extraction of the above-threshold parameters.

A satisfactory fit of the simulated data to the experimental data is very difficult to obtain due to the high number of parameters used in Level 15, as shown in the Appendix. Therefore the known factors, such as overlap capacitance, dielectric constant of the oxide and the substrate layer, the oxide thickness, the substrate layer, and the zero-bias leakage current, were initially fixed [46]. A simultaneous optimization technique was used to extract other model parameters.

In all studies, the experimental transfer curves of the devices were well produced by modifying the AIM-SPICE level 15 [45-47].

2.7 Summary

In this chapter, the structure of oxide thin films and the role of defects on the electrical and optical properties of these devices are briefly discussed. GSZO TFT has the potential of satisfying all the requirements to be used in display technology. In addition, as a wide band gap material (3.3 eV), GSZO is transparent in the visible region and less light sensitive, and can be deposited at low temperatures (< 200 °C), which make GSZO TFT a very promising device for low-cost alternate to the IGZO material system. Other important criteria such as device stability and dynamic characteristics have not been well addressed for GZSO TFTs as shown in Table 4.

Table 4

Comparison of a-Si:H, IGZO, and GSZO TFTs

TFT Semiconductors Materials	**a-Si:H**	**IGZO**	**GSZO**
Microstructure	amorphous	amorphous	amorphous
Fabrication cost	Low	Low	Low
Processing temperature	~250°C	RT - 360°C	< 200°C
TFT Uniformity	good	good	under investigation
Field effect mobility ($cm^2V^{-1}s^{-1}$)	~1	~10 - 30	10^{-3} - 18
On-Off ratio	~10^6	> 10^8	10^3 - 10^7
Long term Electrical Stability	poor	good in dark	under investigation
Long term Optical Stability	poor	better than a-Si	under investigation
Device type	n-MOS	n-MOS	n-MOS

In this work, the stability of GSZO thin films transistors was investigated and the mechanism underlying the variation of their electrical and optical properties is reported.

CHAPTER 3

Methodology

The following chapter is a brief description of the preparation of the GSZO TFTs and information regarding the characterization techniques used. The fabrication techniques used in this work was RF magnetron sputter deposition. Thin-film characterization techniques are discussed including, x-ray reflectivity, device electrical parameter extraction, and optical transmission. The stability procedure is explained including, electrical bias stability and optical stability. Finally, the extraction procedure of the GSZO transfer characteristic using Aim-SPICE simulation is discussed.

3.1 Preparation of GSZO TFTs

All tests were performed on GSZO channel of the TFTs that were produced by RF magnetron sputter deposition with channel layer and oxide layer thickness ranging from 8-15 nm and 65-130 nm, respectively on SiO_2/Si substrates. The growth conditions included different atmosphere pressures ranging from 1-10 mTorr, oxygen flows ranging from 2-10 sccm, and at two annealing temperatures of 140°C and 450°C. For XRR analysis, the GSZO films were deposited on SiO_2/Si substrates with no masks. For absorptance measurement the thin film were deposited on 7059 glass.

3.2 X-ray Reflectivity

X-ray reflectivity (XRR) measurements were performed using CuKα radiation at a wavelength of $\lambda = 0.154$ nm, accelerated voltage of 40 kV, and current of 20 mA (Bruker D8 Diffractometer). A rocking curve method was used to align the x-ray beam for maximum intensity by optimizing the parameters of the Z and Chi positions as shown in Figure 11. The knife-edge collimator enables the removal of the footprint effect by making the probed area

smaller. Slits aid in changing the resolution; a good resolution can be obtained from 0.1-0.2 mm. The intensity of the x-rays reflected from the surface was recorded as a function of incident angle. Measurements were obtained from the rough estimation:

$$d \approx \lambda/2\Delta\theta \qquad (3.1)$$

The obtained data were fitted using the DiffractPlus LEPTOS software to estimate the structural parameters, such as the thickness, roughness, and the density of the layers in the thin films. The roughness of the films obtained was then compared with the atomic force microscopy (AFM) to verify the accuracy of the analysis.

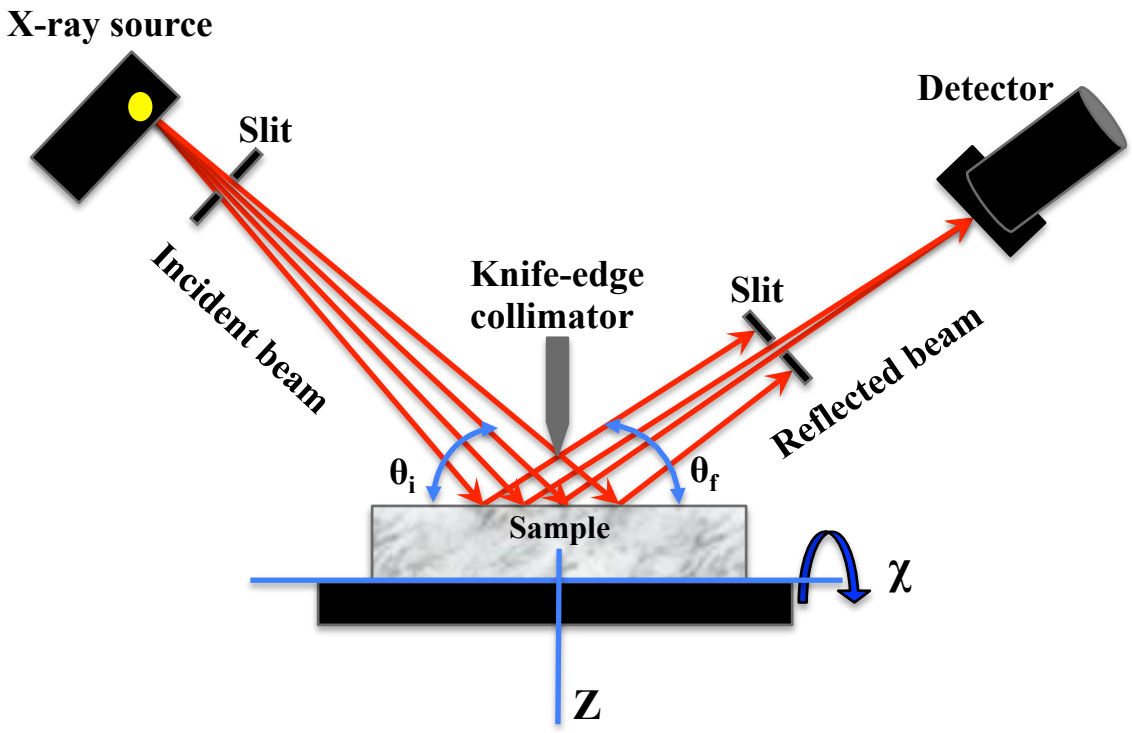

Figure 11. Illustration of the XRR setup.

3.3 Device Electrical Parameter Extraction

To determine the device performance, characterization of the GSZO TFTs' figure of merits is extracted by measuring the transfer characteristics. These figure of merits include: turn

on voltage V_{ON}, the field effect mobility μ_{FE}, saturation mobility μ_{SAT}, subthreshold swing SS, drain off current I_{OFF}, and drain current on-off ratio I_{ON}/I_{OFF}..

V_{ON} is defined as the corresponding gate voltage that brings 5 pA of drain current. At this point there is a sharp increase in the channel conduction, which corresponds to the formation of the accumulation layer. Figure 12. shows extrapolation technique for Von extraction.

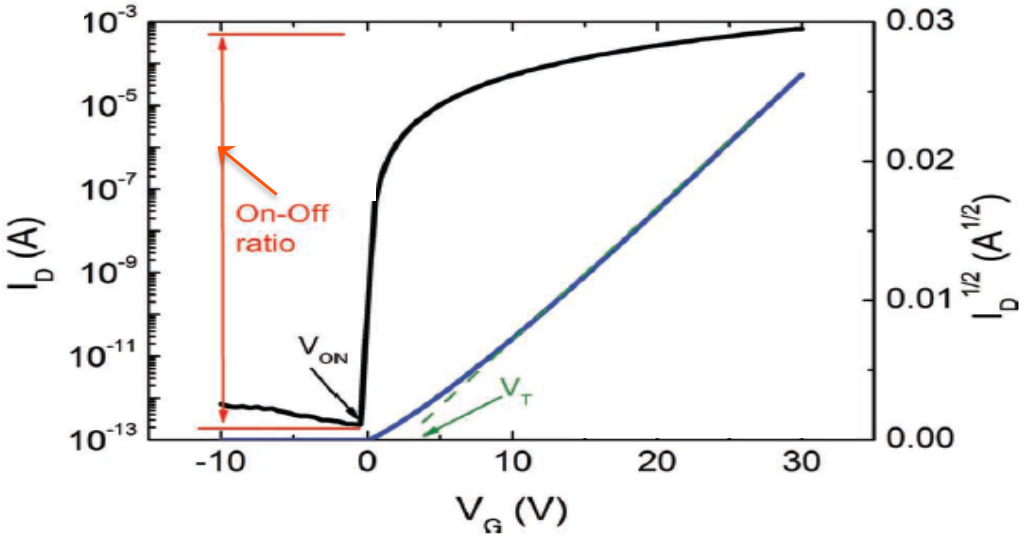

Figure 12. Typical transfer characteristics of a GSZO TFT.

Field-effect mobility μ_{FE} was determined from the linear region of the I_D vs. V_{GS} plot corresponding to the low value of V_{DS} using the following equation:

$$\mu_{FE} = \frac{g_m}{\frac{W}{L} C_{OX} V_{DS}} \qquad (3.1)$$

where g_m is the transconductance ($g_m = dI_D/dV_{GS}$), W and L are channel width and length, respectively, C_{OX} is the gate insulator capacitance per unit area (2.8 x 10^{-8} F), and V_{DS} is fixed.

The saturation mobility μ_{SAT} was determined from the saturation regime of the $I_D^{1/2}$ vs. V_{GS} plot for high V_{DS} using the following equation:

$$\mu_{SAT} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2}{\frac{1}{2} C_{OX} \frac{W}{L}} \quad (3.2)$$

The subthreshold voltage SS gives a measure of the increase in gate voltage required to switch the transistor from an off-state to an on-state by an order of magnitude. A small SS value is desirable because it corresponds to a fast transition. SS is extracted at the steepest point of the log (I_D) – V_{GS} plot by using the following relation:

$$SS = \left(\frac{d \log (I_D)}{d V_{GS}}\right)^{-1} \quad (3.3)$$

The SS values was also used to provide the density of total trap states (N_T) near the channel/insulator interface by the following equation:

$$N_T = \left(\left(\frac{SS\ log(e)}{kT/q}\right) - 1\right)\frac{C_{OX}}{q} \quad (3.4)$$

where *e* is the Euler's number (irrational constant), k is the Boltzmann constant, T is the absolute temperature, and *q* is the charge of an electron.

Lastly, I_{ON}/I_{OFF} is simply the ratio of the maximum to minimum drain current, where the maximum I_{ON} depends on the effectiveness of the semiconductor material, and I_{OFF} depends on the noise level of measurement equipment or gate leakage current.

All TFTs were examined using I-V and C-V measurements. The details of the I-V and C-V set up are provided in Tanina's dissertation [5] and Olanrewaju Ogedengbe's thesis [48].

3.4 Optical Transmission

The optical properties of the thin films were measured with a UV/VIS/NIR spectrophotometer with double beam in the transmission range of 200 - 1000 nm. The absorption data was determined from a Tauc plot of the transmission spectra.

3.5 Stability Procedure

For all stress conditions, the transfer characteristics of the devices were measured under room temperature and under a dark state using the Keithley 4200-SCS and SemiProbe LA-150 probe station. The transfer characteristics were measured at a specific drain voltage, with a grounded source, while sweeping the gate voltage from -20 to 20V at 1 V intervals. A stress voltage V_{ST} of 15 V was applied to the gate, while shorting the source and drain electrodes for a prolonged period of time. A schematic illustration is shown in Figure 13. A fresh, unstressed device was used for each stressing condition. Bias stressing was interrupted at predetermined times in order to measure the transfer characteristics.

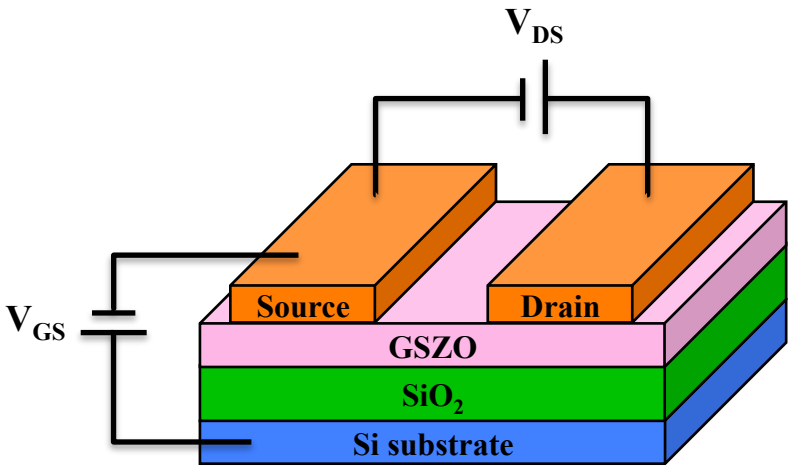

Figure 13. Schematic illustration of GSZO TFT

3.5.1 Electrical stability. The transfer characteristics at initial state and after applying a gate bias stress were investigated to understand the degradation mechanism. A positive bias stress (PBS) and a negative bias (NBS) were applied to the gate for 10^4 s (approximately 3 hrs.). For electrical stability, the transfer characteristics were measured at a V_{DS} = 0.5 V. For PBS, recovery was measured for 1 week.

3.5.2 Optical stability. Photo-excitation was provided by a MicroHR monochromator and a white halogen lamp in combination with an optical fiber (2mm diameter, 6ft long). Measurements were carried out by isolating the external light using a shielding box, as shown in Figure 14. For optical stability study, the response of GSZO TFTs to three critical wavelengths (red at 650 nm, green at 550 nm, and ultraviolet at 410 nm) was investigated. Although the relative intensities of red, green, and ultraviolet light are slightly different, the integrated intensity was calibrated to be approximately 0.72 lux in order to avoid to potential artifacts on the degradation. For measuring the effect of illumination stress, devices were exposed to wavelength of 550 nm with no bias and with a positive and negative bias. The maximum time duration for stress was 10^3 s (approximately 2 hrs.). Degradation of the device characteristics was checked by measuring the transfer characteristics at initial state, during the illumination (at 600 s, 3600 s, and 7200 s), and after illumination at V_{DS} = 10 V. The analysis of the optical stability using the I-V characteristics was verified with corresponding capacitance-voltage characteristics.

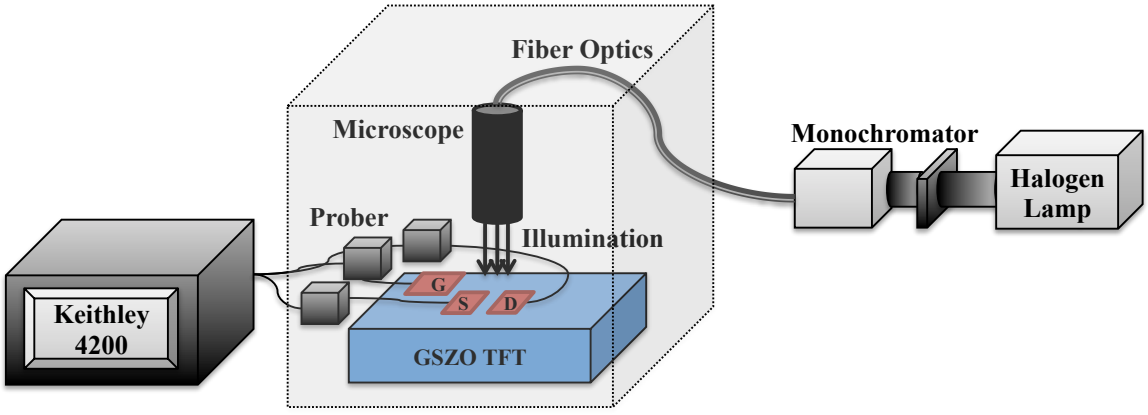

Figure 14. Schematic diagram of the experimental equipment used in this study

3.6 Extraction Procedure Using a-Si:H TFT Level 15 Model in AIM-Spice.

The AIM-Spice Level 15 a-Si TFT model was used to simulate the GSZO TFTs transfer characteristics. Using approximation, the drain current can be obtained from the basic features of this model using the parameters shown in the Appendix.

By varying some of these parameters individually, it can be observed which region is most impacted by a certain parameter as shown in Figure 15 and 16. From this observation, the experimental data can be simulated accordingly**.** The technological data used in the simulation is included in Table 5.

Table 5

Technological parameters used in Aim-Spice simulation

Technological parameters	GSZO TFT
Gate thickness (nm)	130
Intrinsic layer thickness (nm)	15
W (μm)	100
L (μm)	25

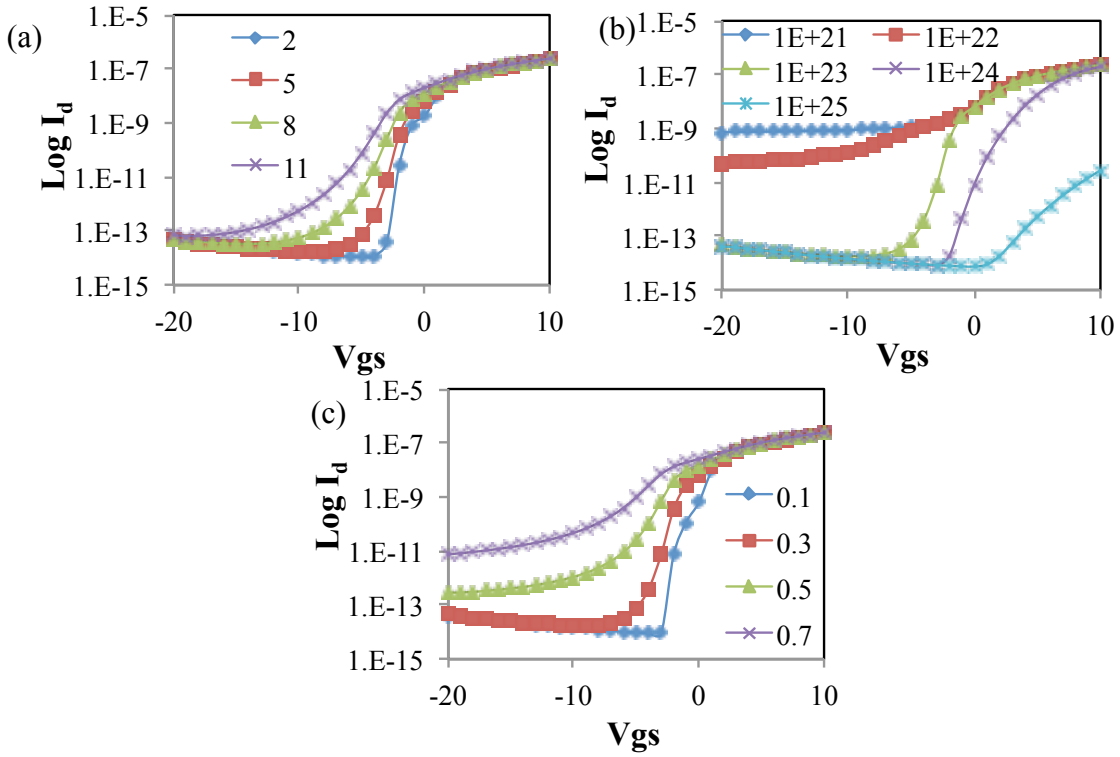

Figure 15. Parameters affect on the below-threshold region: (a) delta, (b) gmin, and (c) vmin.

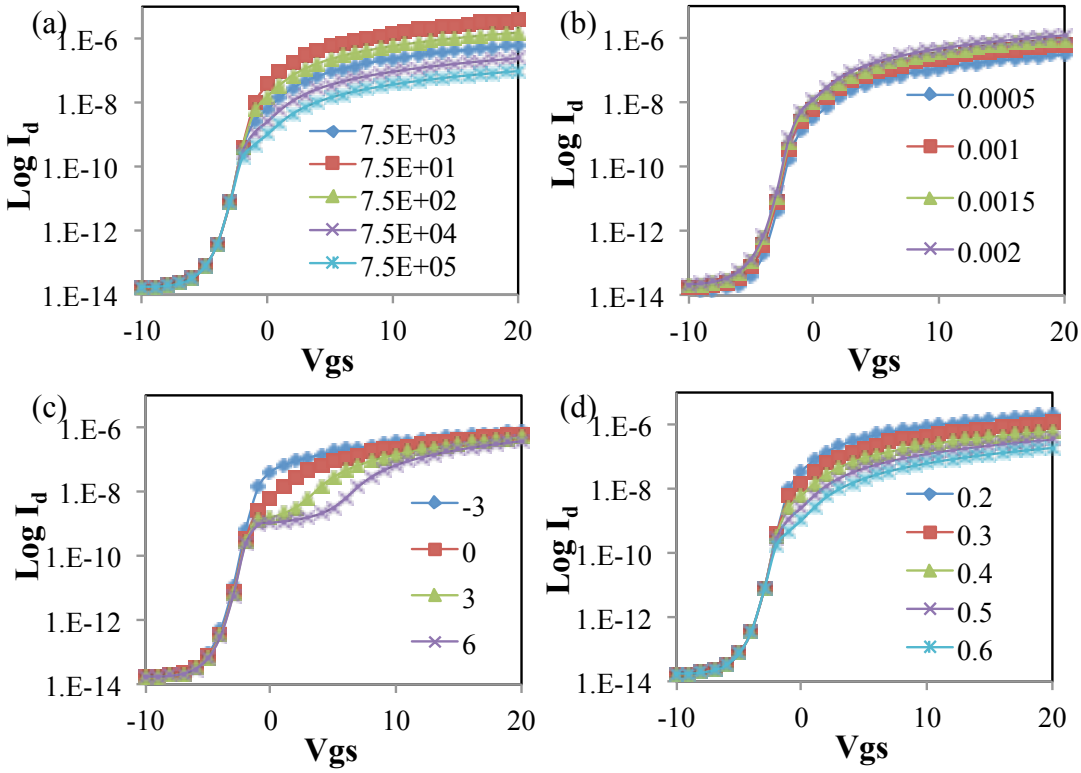

Figure 16. Parameters that affect the above-threshold region: (a) vaa, (b) muband, (c) vto, and (d) gamma.

CHAPTER 4

Results

The chapter presents the results obtained from XRR analysis on unannealed and 350°C annealed GSZO TFTs. XRR and AFM trends observed in 140°C annealed devices with varying pressures from 5-10 mTorr and a 350°C annealed device are briefly discussed. The effect of a positive bias stress (PBS) on different fabrication conditions including, thickness, pressure, and temperature are revealed. The application of stretched exponential equation to extract the time constant of trapping and detrapping during PBS is presented. The results on 140°C annealed devices and 450°C annealed devices (for 1 hr each) under electrical bias and optical stability are also discussed. Finally, the simulation results are obtained using Aim-SPICE.

4.1 XRR Analysis Results

The microstructure characteristics of the GSZO thin films were measured and simulated using XRR and LEPTOS. It provides the density of the active layer of an unannealed thin film to be 5.5 g/cm^3, which is ~2% smaller than that of an 350°C annealed GSZO thin film, which was 5.6 g/cm^3. The measurements of the XRR spectrum and the fitting data of the thickness, surface roughness, and density for these samples are shown in Figure 17. and Table 6, respectively. The experimental values for all samples were within ± 5% of the expected values for the thickness, as estimated from ellipsometry.

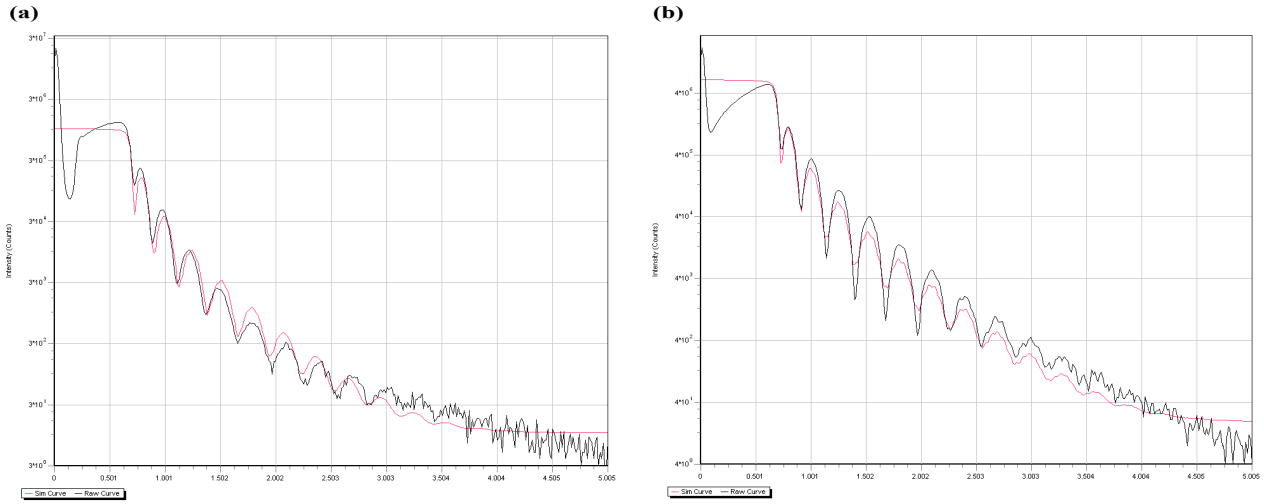

Figure 17. XRR spectrum of (a) unannealed and (b) 350°C annealed GSZO TFTs.

Table 6

X-ray reflectivity data of unannealed and 350°C annealed TFTs

Sample	SiO_2 layer thickness(nm)	ZnO layer thickness (nm)	SiO_2 layer roughness (nm)	ZnO layer roughness (nm)	ZnO density ($g \cdot cm^{-3}$)
Unannealed	122.7975	28.9398	0.9564	0.6858	5.5099
350°C Annealed	123.0566	28.6258	0.9401	0.6511	5.61475

The critical angle for reflection of the annealed thin film is higher than that of the unannealed thin film, indicating that the annealed sample was denser than the unannealed thin film. In addition, the trends exhibited in the thin film are as follows:

a) Surface roughness: the active layer of unannealed sample > annealed sample

b) Film Density: the active layer of unannealed sample < annealed sample

AFM topographs of GSZO thin films at various deposition conditions are shown in Figure 18. The surface roughness values of 140°C annealed (5 and 7 mtorr) samples are greater than the 350°C annealed sample as shown in Table 7. Exception of 10 mtorr, which is possibly due to the

small thickness of the active layer. However, this tendency is consistence with the XRR fitting results.

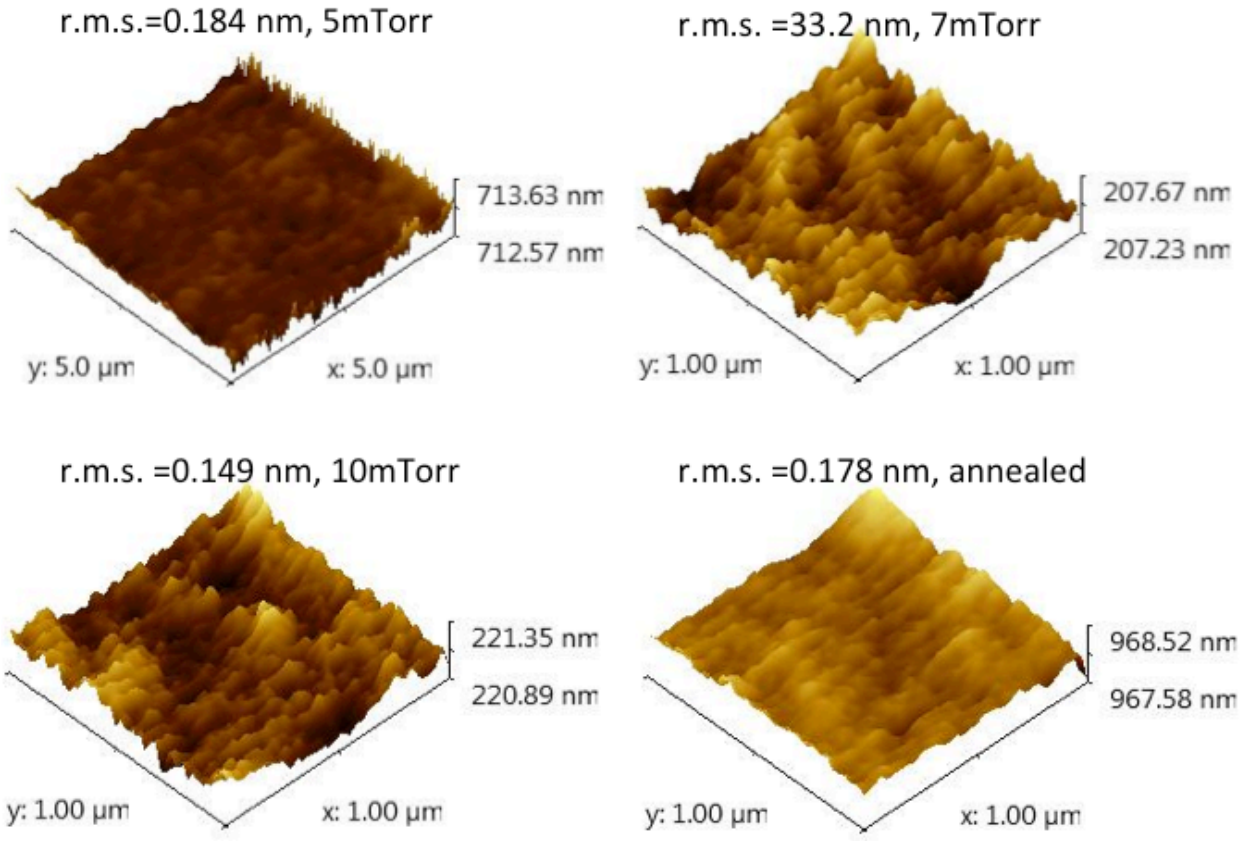

Figure 18. AFM topographs of GSZO thin films.

Table 7

The XRR data compared with AFM data

Sample	Thickness (nm)	Surface Roughness (nm)	Density (g·cm^{-3})	Roughness r.m.s (nm)
140°C 5mTorr	26.868	1.5751	4.581	0.184
140°C 7mTorr	13.084	0.7782	5.282	33.2
140°C 10mTorr	10.956	0.5972	6.96	0.149
350°C Annealed	15.949	0.4862	5.512	0.178

4.2 Electrical Stability Results

4.2.1 Effect of channel/insulator thickness. The effects of channel and gate thickness on the electrical properties during the positive bias stress-induced stability were measured. The shift in the transfer curve decreases when the channel thickness increases from 10 to 15 nm at 140°C, as shown in Figure 19. Using Eq. (3.4), the total trap states with channel layer thickness of 10 and 15 nm were estimated to be 3.24 x 10^{12} and 3.28 x 10^{12} cm^{-2}, respectively. For the oxide thickness of 65 nm and 123 nm, N_T was ~4 x10^{12} /cm^2, and increased to approximately 10^{13}/cm^2, as shown in Table 8. The mobility increased with increasing layer thickness for both channel and oxide.

Table 8

Total trap density and mobility of TFTs with different channel/gate thickness

Sample		μ_{FE} (cm^2/V-s)	N_T (cm^{-2})
Channel layer thickness	10	0.041	3.25E+12
	15	0.786	3.28E+12
Gate insulator thickness	65	0.279	4.27E+12
	123	0.786	3.10E+12
	130	2.061	1.66E+13

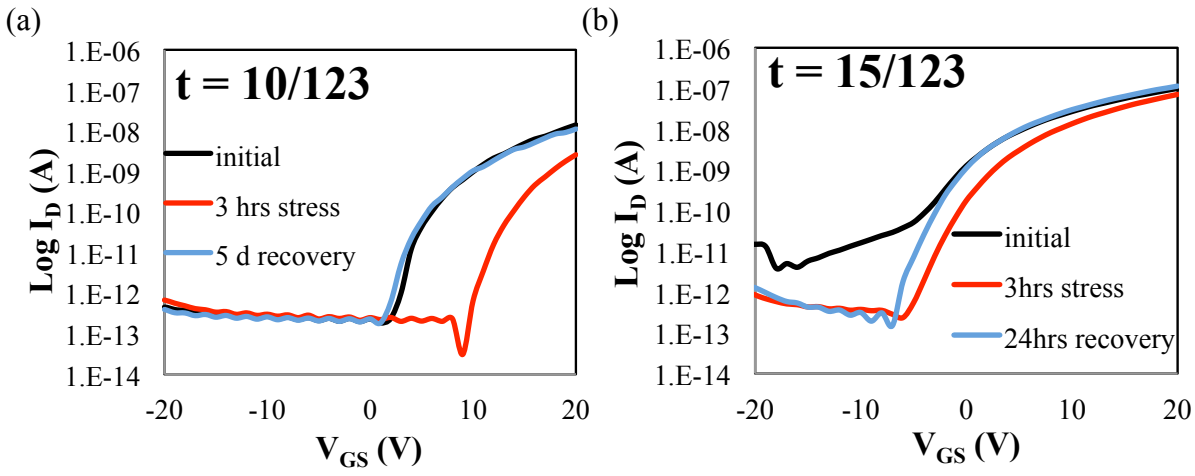

Figure 19. Transfer characteristics of GSZO TFTs with channel thickness of (a) 10 and (b) 15nm under PBS for 3hrs.

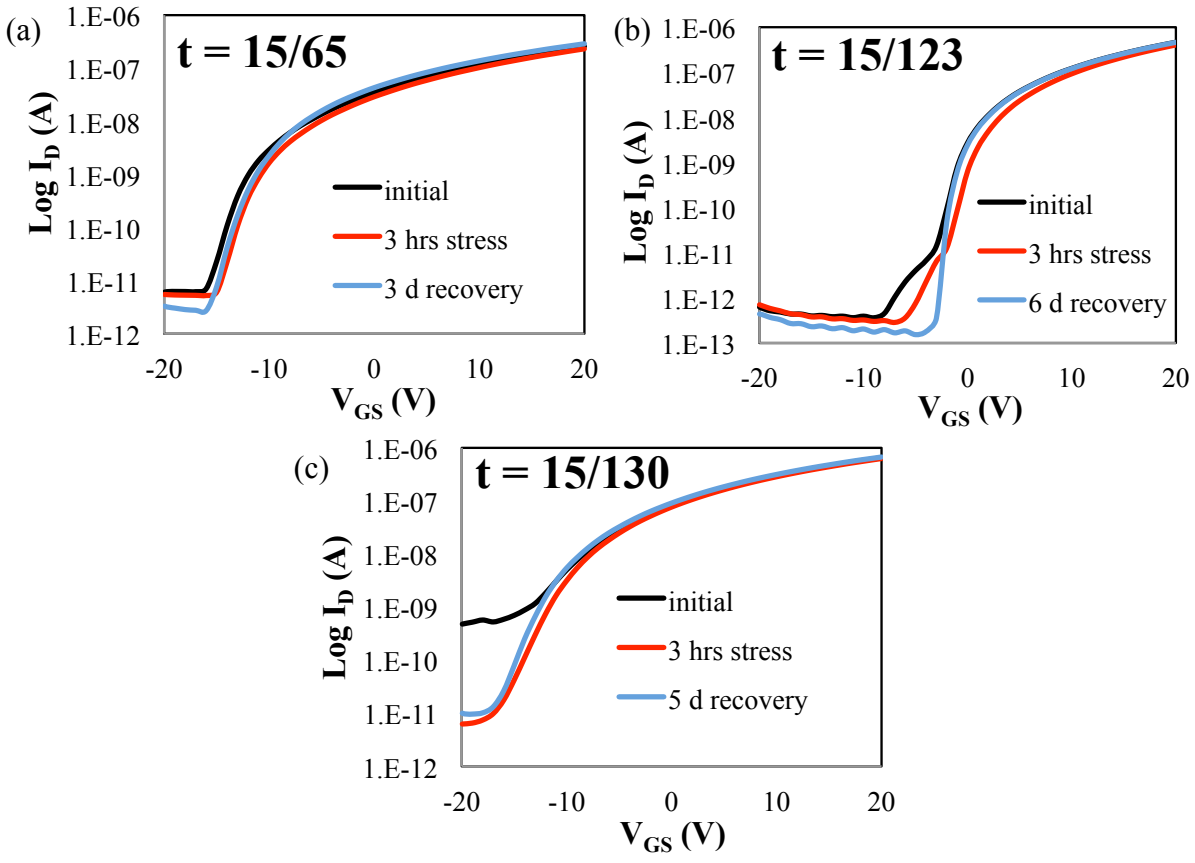

Figure 20. Transfer characteristics of GSZO TFTs with oxide thickness of (a) 65, (b) 123, and (c) 130 nm under PBS for 3hrs.

4.2.2 Effect of pressure. The effect of deposition pressure at 1, 5, and 10 mTorr on the transfer characteristics of the GSZO thin films post annealed at 140°C was measured for a period of 3 hrs. (10^4 s), as shown in Figure 21. All the TFTs tested exhibit the following: a) a positive transfer curve shift; b) a stable mobility over the entire stress duration; c) slight degradation in the SS (~ΔSS= 0.4); d) recovery of the transfer curve toward the initial state, with an exception to the 1 mTorr which didn't fully recover.

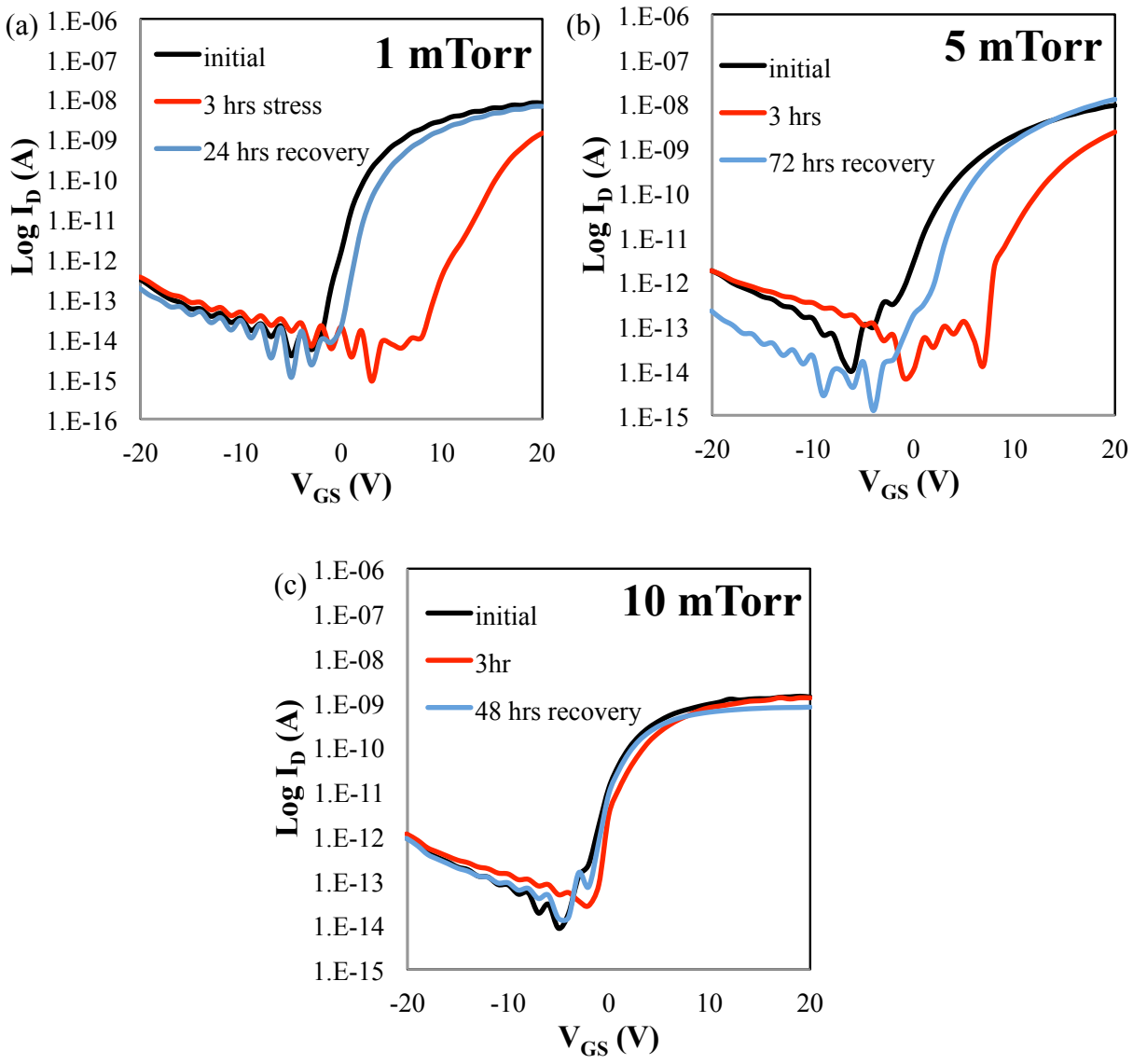

Figure 21. Transfer characteristics of GSZO TFTs with deposition pressures of (a) 1, (b) 5, and (c) 10 mTorr under PBS for 2h.

4.2.3 Effect of temperature. Constant voltage bias stress measurements were performed for a period of 3 hrs. (10^4 s) on GSZO thin film transistors fabricated using a post-deposition annealing temperature of 140°C, 350°C, and 450°C. All the TFTs tested exhibit the following: a) a positive transfer curve shift; b) a continuous decrease in mobility over the entire stress duration; and c) recovery of the transfer curve toward the initial state. The TFTs subjected to a

higher annealing temperature are more stable, as shown in Figure 22. The results in Table 9. indicated that an improved interface between the channel layer and gate insulator can be achieved by annealing at 350°C, which had the least number of interface traps N_{it}. TFTs annealed at 140°C exhibited the most degradation but had full recovery within 1 week (135 hrs.).

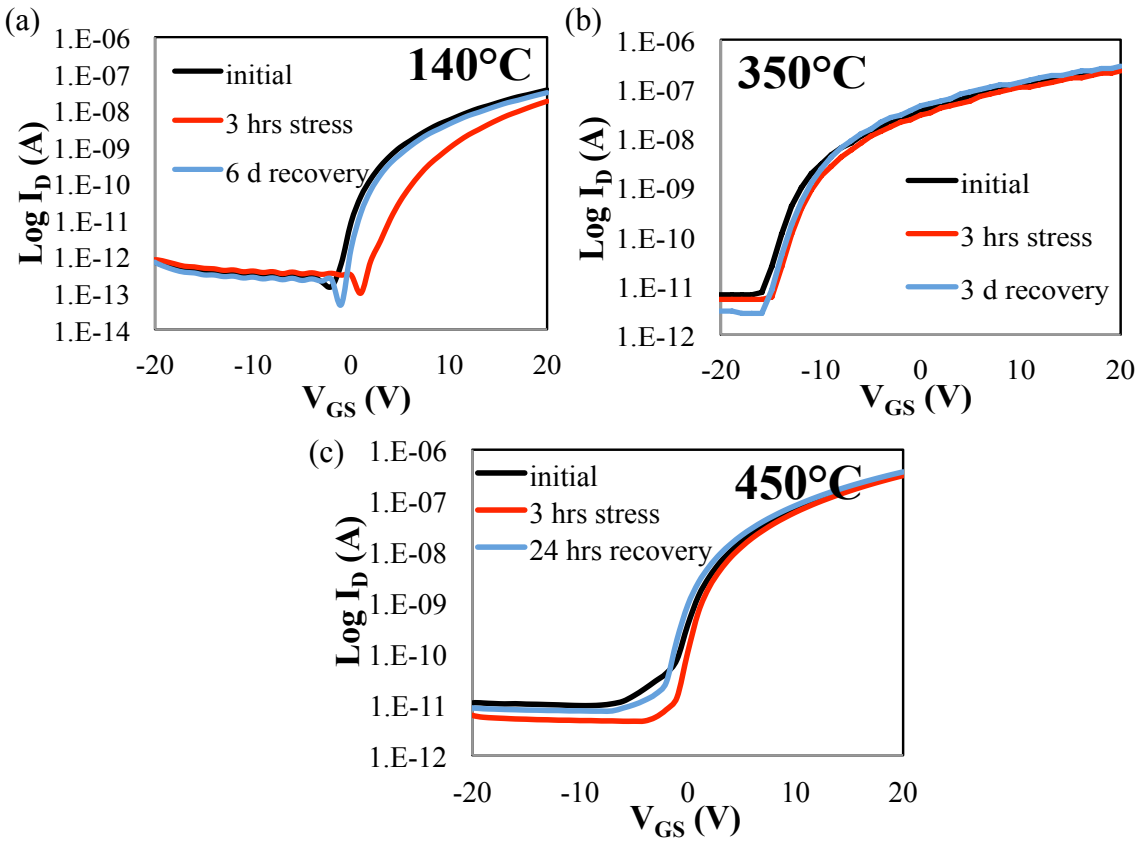

Figure 22. Transfer characteristics for GSZO TFTs annealed at different temperatures: (a) 140°C, (b) 350°C, and (c) 450°C.

Table 9

Electrical characteristics of TFTs annealed at different temperatures

Sample (°C)	V_{ON} (V)	I_{ON}/I_{OFF}	SS (V/decade)	μ_{FE} (cm^2/V-s)	N_{it} (cm^{-2})
140	1	2.41E+05	0.89	8.02E-02	1.61E+12
350	-16	4.69E+04	0.34	2.79E-01	4.24E+11
450	-6	4.35E+04	0.49	7.36E-01	2.97E+12

4.2.4 Positive and negative gate assessment of GSZO TFTs. The effect of a positive gate bias stress shifts the transfer curve to the right, while a negative gate bias stress shifts the curve to the left for a GSZO TFT annealed at 140°C, as shown in Figure 23. The transfer curve shift during the positive gate bias stress is generally greater than that of the negative gate bias stress.

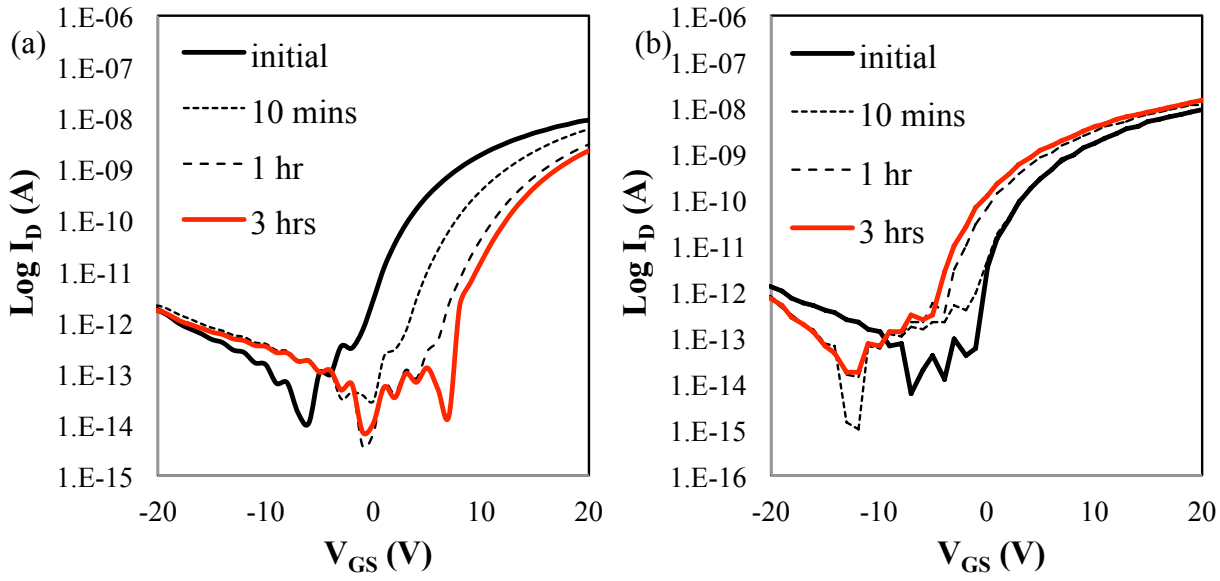

Figure 23. Typical instability of GSZO TFT transfer characteristics under a (a) positive and (b) negative gate bias stress measured for V_{DS} = 0.5 V.

4.2.4.1 Effect of positive gate bias stress. The variation in the figure of merits during the positive gate bias stress is observed in Figure 24-25. The V_{ON} of GSZO transistors under dark conditions was positively shifted after the application of PBS for 3 hrs. Under the PBS

application, it can be seen that V_{ON} increases and the stability increases for the TFT with a higher pressure and higher annealing temperature. The TFT with large positive V_{ON} values corresponds to the TFT that is strongly influenced by the trapping in interface states and/or bulk traps in the channel band gap, thus has the worst stability.

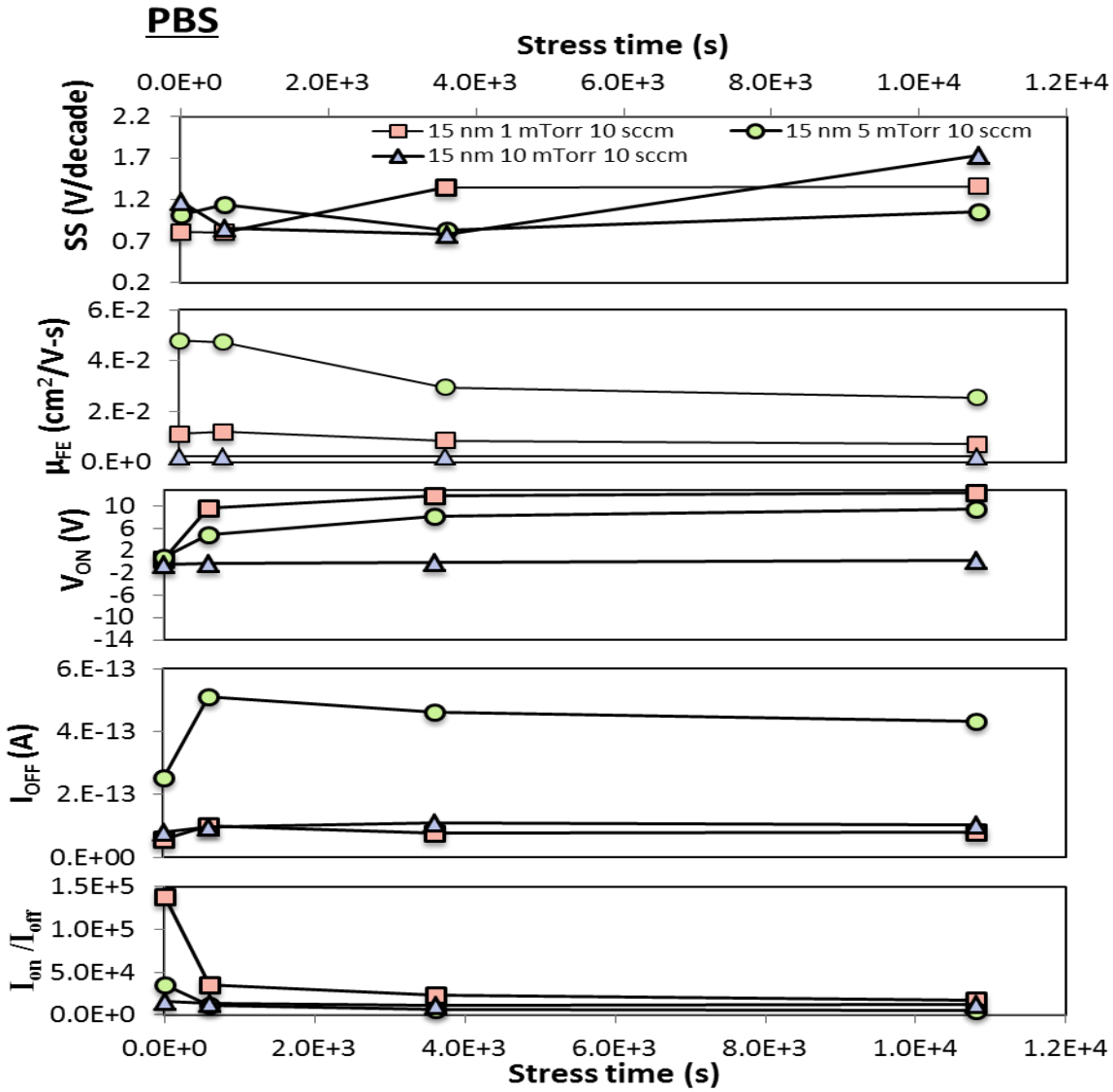

Figure 24. Variations of figure of merits of low temperature deposition of TFTs under positive gate bias stress.

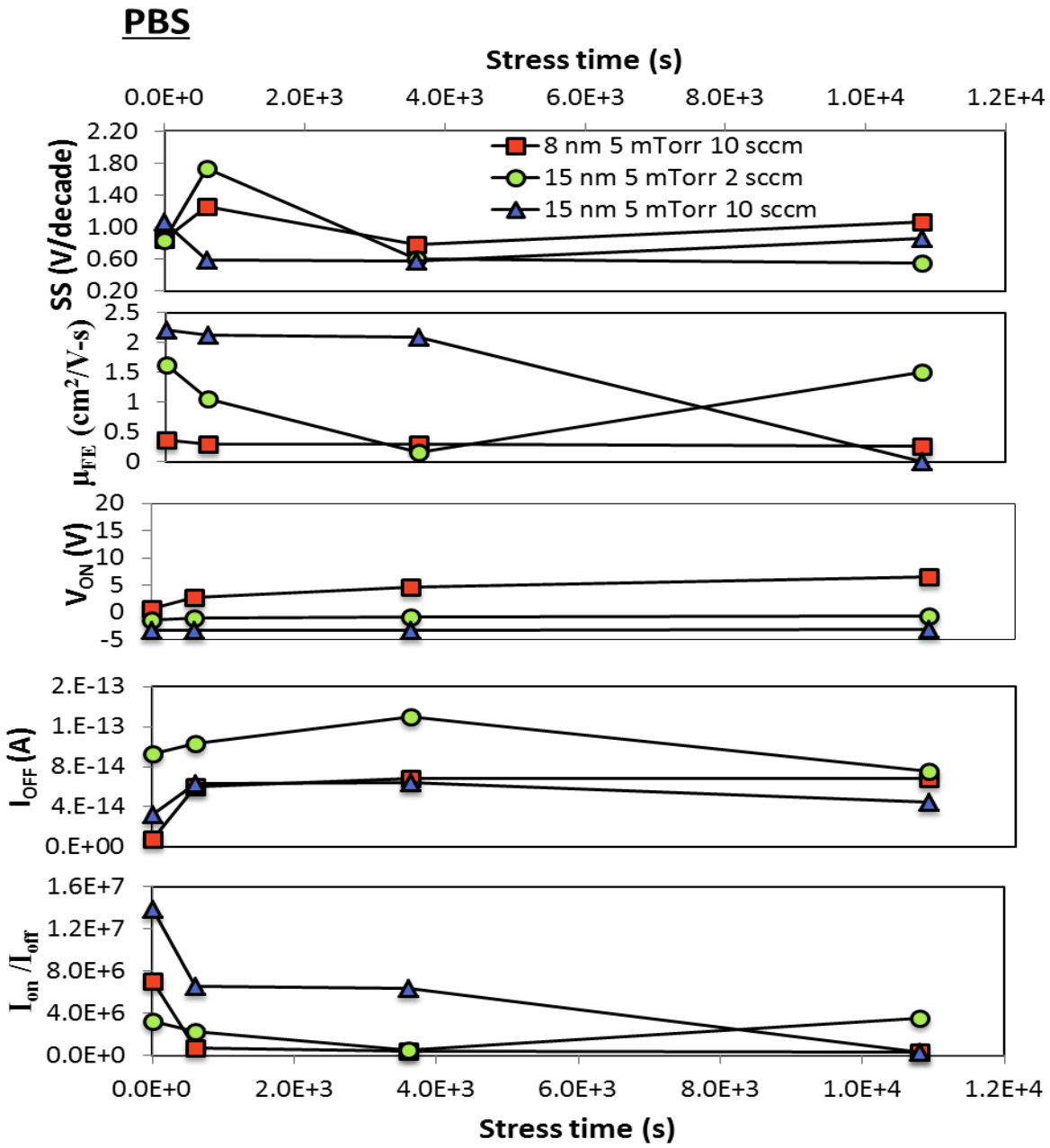

Figure 25. Variations of figure of merits of high temperature deposition of TFTs under positive gate bias stress.

Positive bias stress measurements showed a gradual decrease in ΔV_{ON} (1 mTorr-12 V, 5 mTorr-8.3 V and 10 mTorr-0.75 V) with increasing deposition pressures. The positive shift is due to electron trapping at the gate insulator and/or interface [28]. The more porous 1 mTorr device showed the largest positive V_{ON} shift suggesting it has the highest concentration of

shallow defects. This density of shallow defects decreases with increasing pressure suggesting the lower deposition pressure results in ionization energy too low to form GSZO film with little to no defects. An increase in deposition pressure results in a much more stable GSZO TFT with a ΔV_{ON} of only 0.75 V. The 1 mTorr device also shows a hump in its electrical characteristics which has been reported to be the presence of Zn_I which forms a second path of charge flow [49]. The porous nature of the 1 mTorr device further allowed the transport of Zn_I to the surface of the film after PBS, which thus formed the second current path. The presence of this hump is slightly seen in the 5 mTorr device however cannot be seen in the 10 mTorr device. A gradual increase in film density with deposition pressure from XRR data explains this gradual reduction of hump presence in the transfer I-V characteristics.

4.2.4.2 Effect of negative gate bias stress. The variations in the figure of merits during the negative gate bias stress of GSZO TFTs annealed at 140°C and 450°C is observed in Figure 26-27. The V_{ON} of GSZO transistors under dark conditions was negatively shifted after the application of NBS for 3 hrs. This negative shift is attributed to the band bending resulting in positively charged donor states[50]. Under NBS, free holes are generated in the active region. However, these devices maintained good stability under negative bias stress compared to the instability induced by the PBS which is comparative with literature [51]. There were minor changes in SS, I_{OFF}, and I_{ON}/I_{OFF} as shown in the Figure 26 and 27.

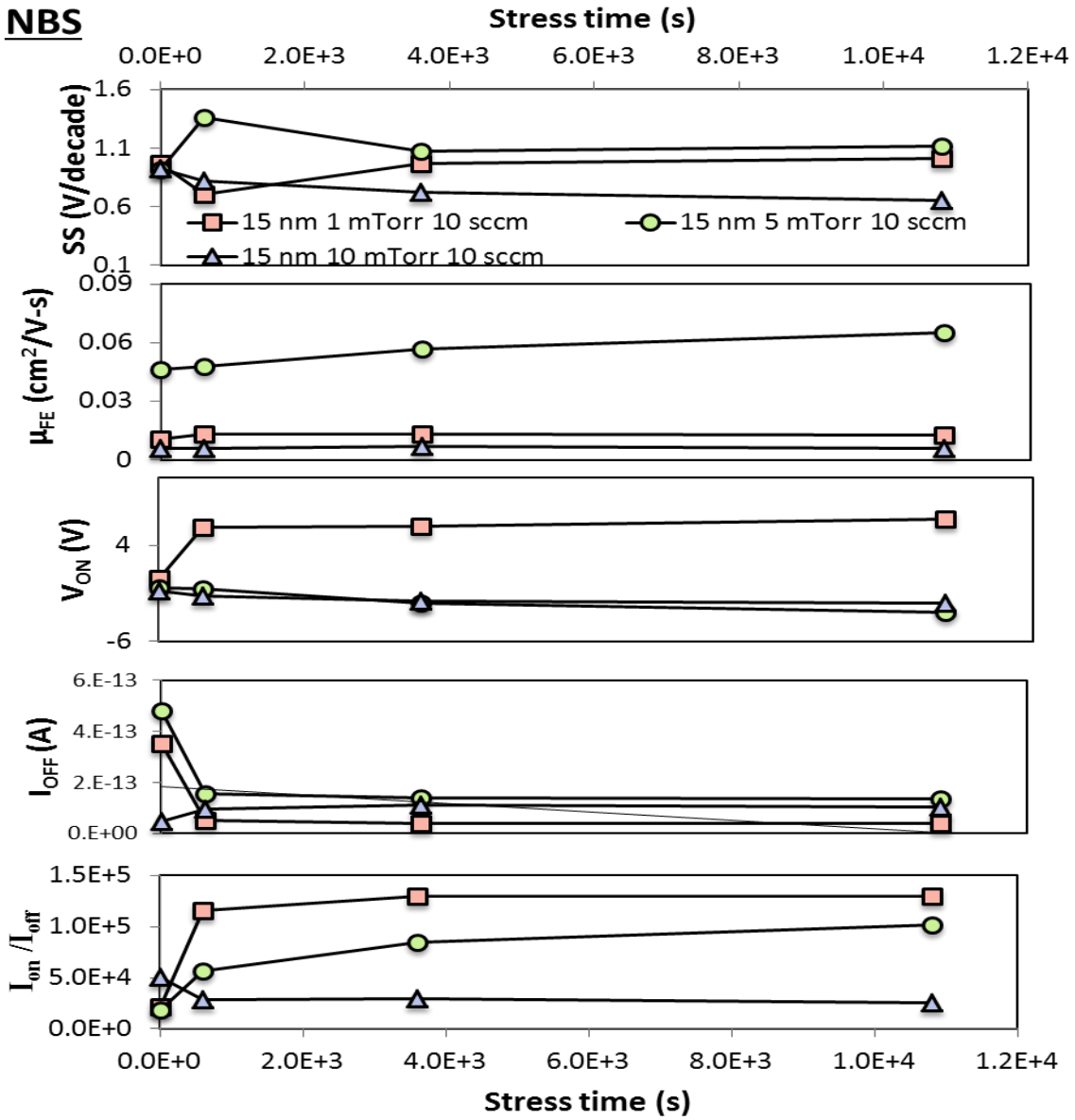

Figure 26. Variations of figure of merits of low temperature deposition TFTs under negative gate bias stress.

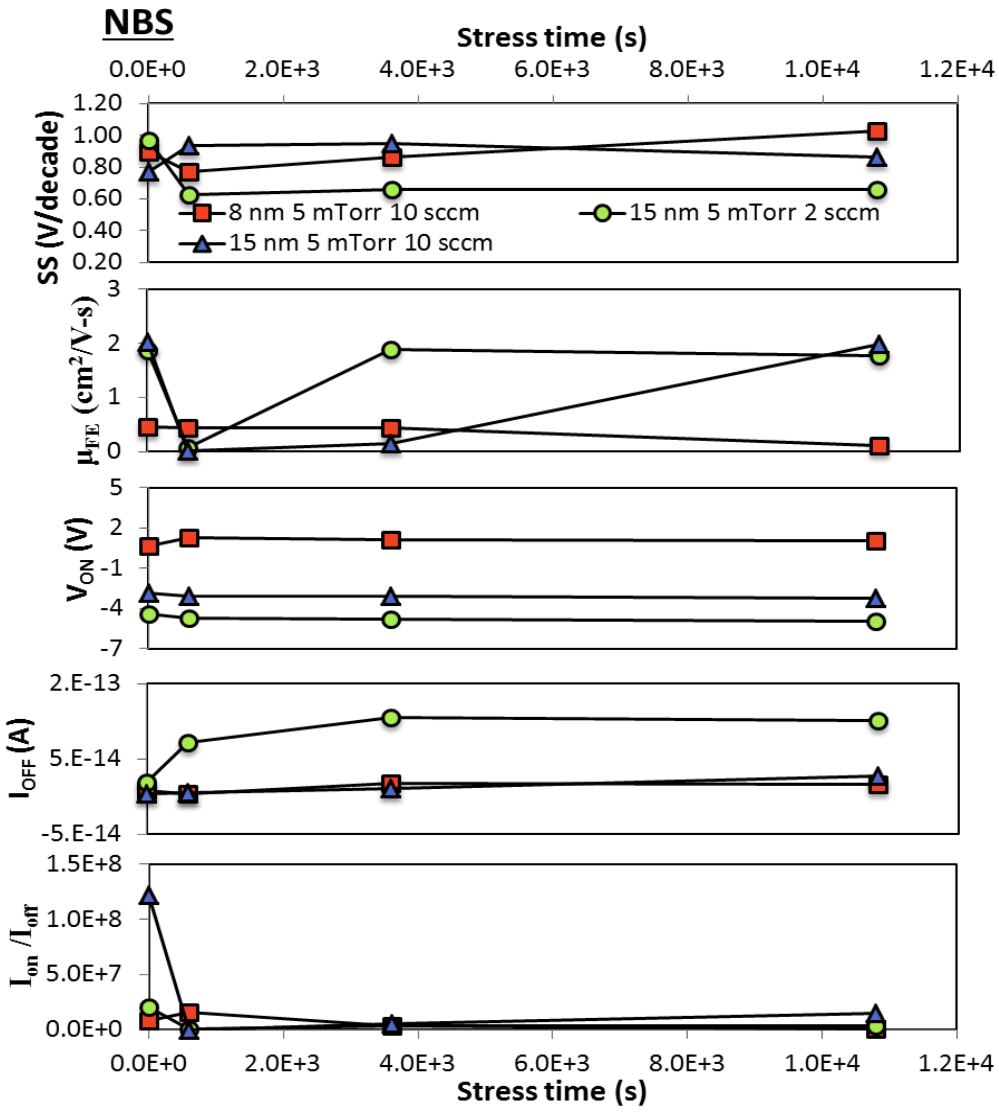

Figure 27. Variations of figure of merits of high temperature deposition of TFTs under negative gate bias stress.

As observe in Figures 24-27, an application of positive and negative gate bias on different TFTs structures for a period of 10^4 s induces instability in the figure of merits. In low temperatures annealed samples, V_{ON} shifts towards the positively during the positive stress and negatively during the negative stress. The μ_{FE} is stable. I_{ON}/I_{OFF} decreases during PBS and increases during NBS due to the increase in I_{OFF}. SS gradually degrades. Exception:

1. V_{ON} is stable for 15 nm 10 mTorr 10 sccm for both stress

2. V_{ON} shifts positively for 15 nm 1 mTorr 10 sccm during NBS
3. I_{OFF} decreases for 1 and 5 mtorr during NBS
4. SS is stable in 15 nm 5 mTorr 10 sccm
5. μ_{FE} gradually decreases during PBS and increases during NBS in 15 nm 5 mTorr 10 sccm.

In the high temperature annealed samples, V_{ON} is quite stable under both positive and negative bias. I_{ON}/I_{OFF} decreases for all samples during the positive gate bias stress and is stable during the negative bias stress. There are no systematic trends in SS and μ_{FE} in thicker channels, however it degrades for all devices during the negative bias stress. The thinner devices are stable under positive gate bias stress and gradually decreases under negative gate bias stress. Exception:

1. SS in 15 nm 5 mTorr 2 sccm improves
2. I_{ON}/I_{OFF} decreases in 15 nm 5 mTorr 10 sccm during NBS.

All other stress variations are shown in the Appendix. Overall the high temperatures samples are more stable than low temperature samples except for 5 mTorr 10 sccm. However the low temperature shows an improvement except for μ_{FE} , which degrades; the largest variation is at 5mTorr. The μ_{FE} is the highest for 5mTorr annealed at 350°C. The device degradation was dominant for PBS.

To clarify the mechanism of the degradation of the PBS and NBS, the energy band diagram during the stress is shown in Figure 28. At initial state, the energy bands are assumed to be at flat-band as shown in Figure 28a. When applying a positive bias to the gate, electrons can accumulate in the insulator/channel interface creating a region of negative charges, which causes the energy bands to curve negatively (downwards), as shown in Figure. 28b. This positive shift could be attributed to various effects including: 1) a fixed positive charge at the gate insulator, 2)

electron trapping at the gate insulator/channel layer and 3) the traps in the bulk of the channel, both due to the positively charge oxygen vacancy, and finally 4) surface back channel interface resulting from enhanced field induced oxygen adsorption at the surface. The first option is ruled out due to the stable thermally oxide grown layer on Si. The last option can also be neglected as all TFTs would have had similar behavior; therefore, this is associated to the trapping of the electrons in the positively charged trap states.

When a negative bias is applied at the gate, the electrons in the channel are depleted of carriers for the charge trapping, thus creating a region of positive charges resulting a positive curve (upwards) of the energy bands, as shown in Figure 28c.

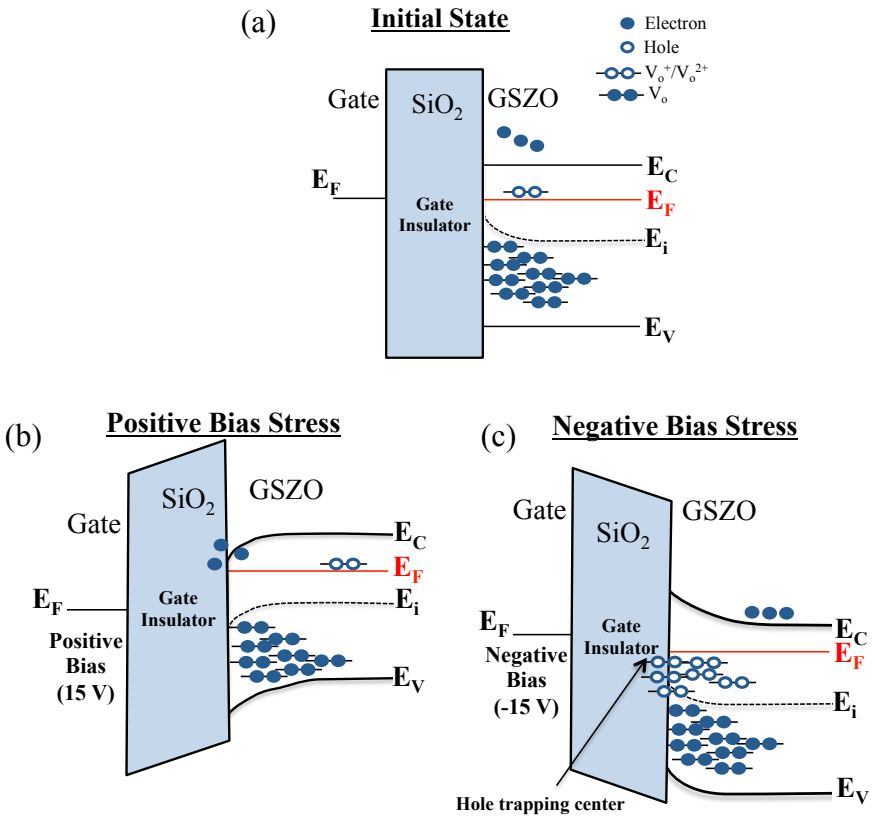

Figure 28. Schematic illustration of energy band diagram of the GSZO TFT (a) at initial state, under (b) PBS stress, and (c) NBS.

4.2.5 Stretched exponential equation. In order to characterize the bias-stress effect, the measure of decay and recovery under an applied positive gate and negative bias was estimated using equation 4.1.

$$\Delta V_{ON} = \Delta V_{ON_0}\{1 - (\exp(-(t/\tau)^{\beta}\} \qquad (4.1)$$

where ΔV_{ON_0} is the ΔV_{ON} at infinite time, β is the stretched-exponential exponent, and τ is the trapping time for the stress phase and detrapping time for recovery phase. The τ has been associated with the duration for which the electrons are trapped or the average time for oxygen adsorption. This equation is a modified version of equation 2.1 where V_{th} was defined the same as the V_{ON} in this work. In our case, the following results can be better explained when τ is considered as the duration associated with the trap rather than oxygen adsorption.

The experimentally obtained results were well fitted by the stretched exponential equation as shown in Figure 29.

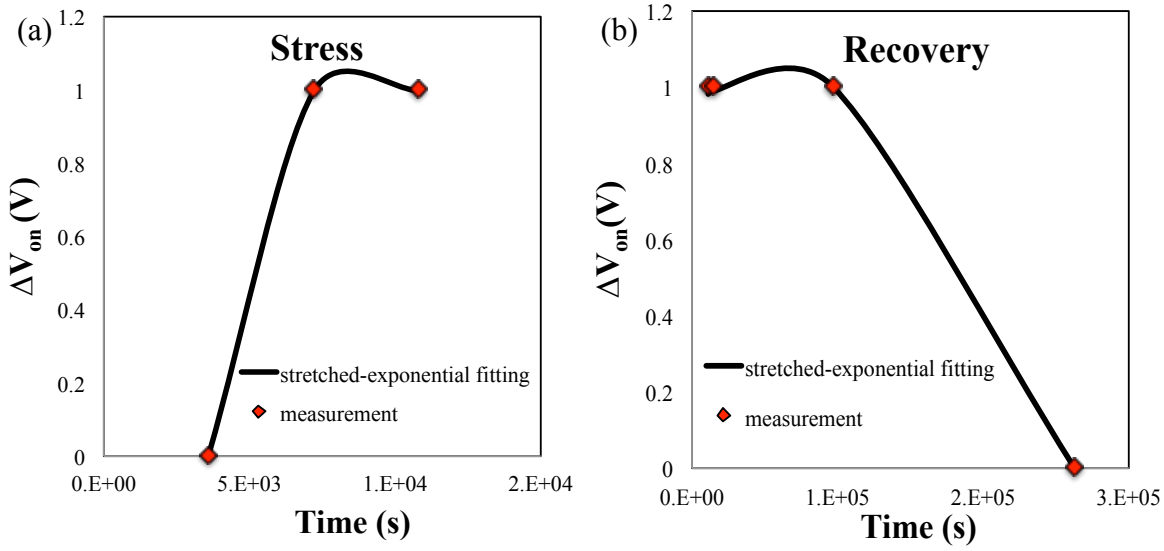

Figure 29. Time evolution of drain-source ΔV_{ON} during (a) stress and (b) recovery phase for a period of 10^4 s.

In Figure 30., the observed trends in the characteristics trapping time are as follows: a) a decrease in τ with a increase in channel thickness; b) an increase in τ with an increase in interface thickness; c) a decrease in τ with an increase in pressure; and d) τ is smaller at 450°C annealed samples (~10^1) than at 140°C annealed samples (~10^2) by 1 order of magnitude. A smaller τ means long term stability. This suggests that post annealing treatment at higher annealing temperature, a thicker channel with thinner interface, and higher pressures improves the stability of a GSZO thin films electrical characteristics.

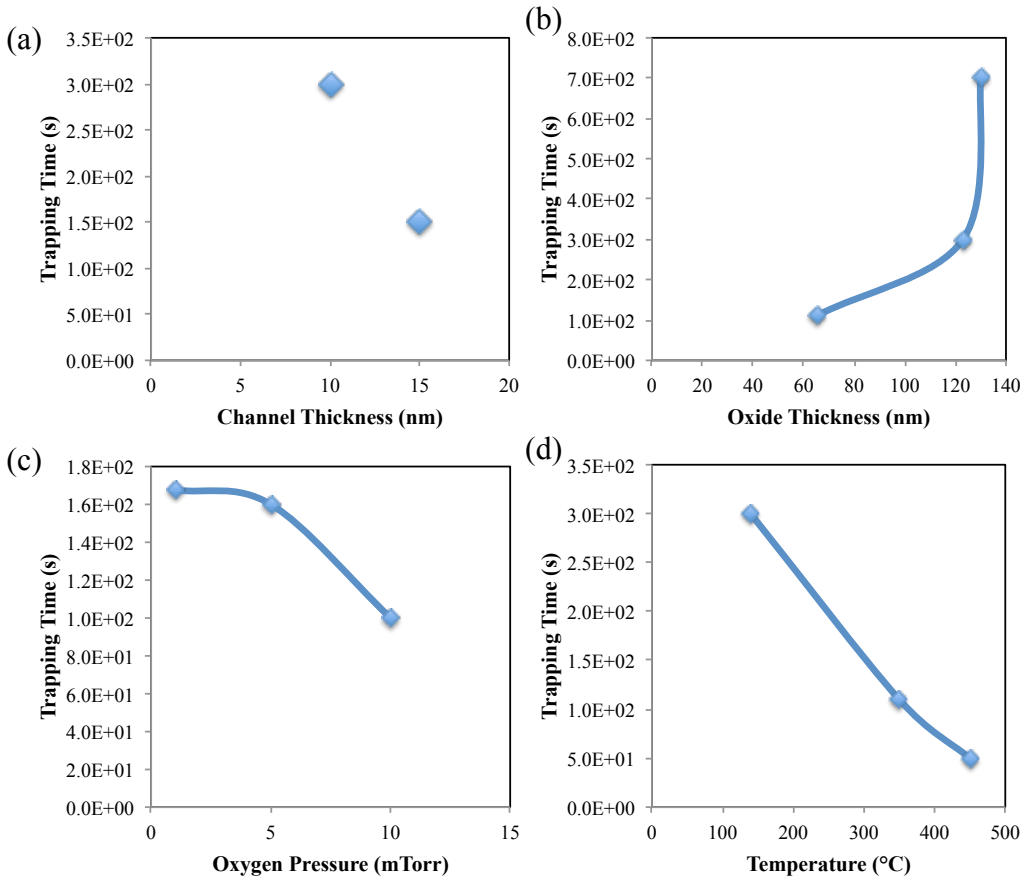

Figure 30. Trapping time dependence on (a) channel thickness, (b) oxide thickness, (c) oxygen pressure, and (d) temperature.

The values determine in our work does compare well with the reported fitting values in literature [16] for ZnO films, which are τ ~10^4 s and β ~ 0.5 for stress and τ ~10^4 s and β ~ 0.2

for recovery, as shown in Table 10. However, a comparison between published works is quite difficult due to the variation of fabrication conditions.

Table 10

Stress and recovery data extracted using the stretched exponential equation

Thickness (t_{ch}/t_{ins})	Condition	Stress/ Recovery	τ (s)	β
15/130	140°C 1 mTorr 10 sccm	Stress	1.7×10^2	0.6
		Recovery	1.4×10^3	0.45
	140°C 5 mTorr 10 sccm	Stress	1.6×10^2	0.6
		Recovery	4.0×10^3	0.5
	140°C 10 mTorr 10 sccm	Stress	1.0×10^2	0.6
		Recovery	1×10^4	0.5
10/123	140°C 10 mTorr 10 sccm	Stress	4.1×10^2	0.58
		Recovery	7.0×10^2	0.6
	140°C 5 mTorrr 10 sccm	Stress	3.0×10^2	0.58
		Recovery	9.1×10^2	0.58
15/123	140°C 10 hr 5 mTorr 10 sccm	Stress	2.0×10^2	0.5
		Recovery	8.0×10^2	0.6
	350°C 10 hr 5 mTorr 10 sccm	Stress	3.0×10^2	0.5
		Recovery	1.2×10^3	0.55
15/130	350°C 5 mTorr 2 sccm	Stress	7.0×10^2	0.5
		Recovery	5.0×10^3	0.56
	350°C 5 mTorr 2 sccm	Stress	1.5×10^3	0.5
		Recovery	4.0×10^2	0.3
15/65	350°C 5 mTorr 2 sccm	Stress	1.1×10^2	0.4
		Recovery	1.0×10^3	0.58
	400°C 5 mTorr 10 sccm	Stress	3.0×10^2	0.53
		Recovery	5.0×10^2	0.52
15/130	450°C multilayer	Stress	2.0×10^2	0.5
		Recovery	3.0×10^2	0.4
	450°C 1hr 5 mTorr 2 sccm	Stress	3.3×10^2	0.5
		Recovery	4.0×10^2	0.4

Table 10

Cont.

15/130	450°C 1hr 5 mTorr 10 sccm	Stress	3.5×10^2	0.5
		Recovery	3.0×10^3	0.4
8/130	450°C 1hr 5 mTorr 10 sccm	Stress	5.0×10^1	0.5
		Recovery	2.0×10^3	0.4

4.3 Optical Stability Results

Figure 31. shows the plot of $(\alpha h\nu)^2$ as a function of photon energy ($h\nu$) for GSZO films. From this plot, it can be seen that the value of the band gap of GSZO thin film increased from 3.21 to 3.25 eV with decreasing the annealing temperature, which is described by the Burstein-Moss shift (BM shift). The BM shift is caused by the filling of excessively charged carriers in the lowest levels of the conduction band and the transitions to energies above the Fermi level. At 450°C: a= 0.171, λ= 269nm, the concentration of free electrons, N_e, is $3.91 \times 10^{16}/cm^3$, and at 140°C: a= 0.193, λ= 251nm, it is $5.04 \times 10^{16}/cm^3$. These values were calculated using equation 2.2, assuming tau and refractive index were 0.25 s and 1.8, respectively. Tau was obtained from the stretched exponential equation during recovery phase, and the refractive index was obtained from ellipsometry [34, 35]. The band gap extracted in study for GSZO TFTs does fall within the range of literature work, which was 3.2 to 3.25 eV [3].

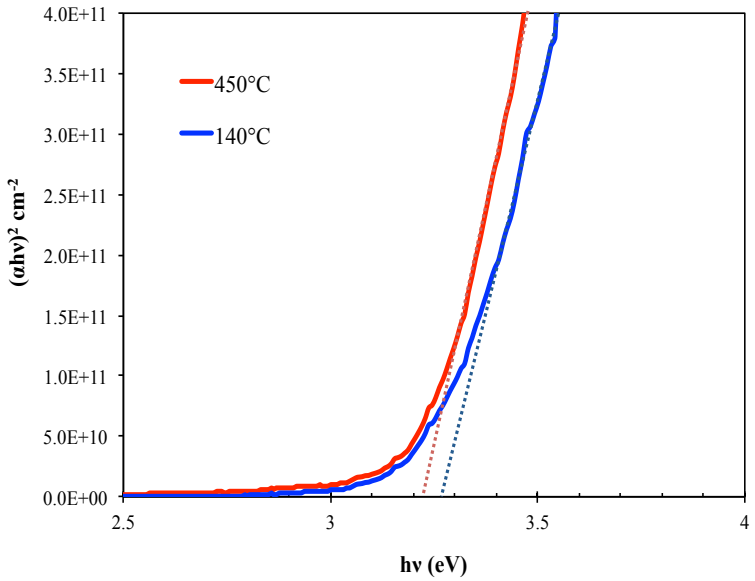

Figure 31. UV absorption spectra of the absorption coefficient squared versus photon energy of GSZO films deposited on glass at 140 and 450°C.

4.3.1 Effect of different wavelengths of light. The effect of different wavelengths of light on the transfer characteristics of GSZO thin films is shown in Figure 32. It was found that a small variation was observed when $\lambda > 500$ nm. However, when exposed to smaller wavelengths ($\lambda < 500$ nm) the most significant changes were observed as shown in Figure 32a, which is due to band-to-band transitions.

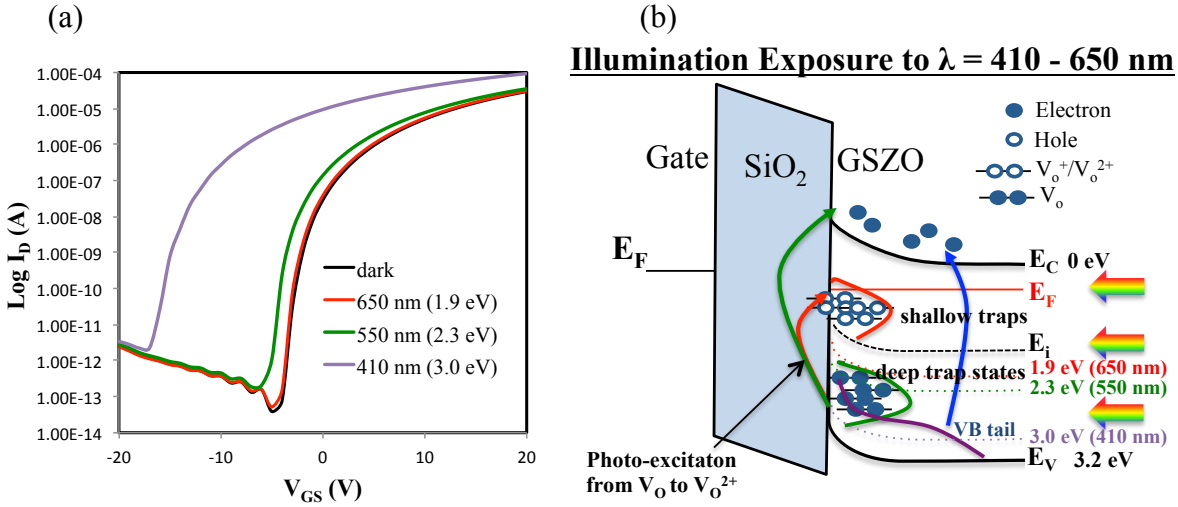

Figure 32. (a) Typical transfer characteristics of GSZO under illumination stress under different wavelengths (650- 410 nm) with no bias for 1hr. (b) Schematic illustration of the photoexcitation

of electrons from V_O and VB tail states under illumination and creation of V_O^{2+} states (410-650nm, E_{photon} 1.9-3.0 eV).

The 650 nm light has photon energy of ~1.9 eV which excites electrons trapped in the CB tail states, shallow traps and mid traps but is too low of energy to excite charges from deep traps as shown in Figure 32b.

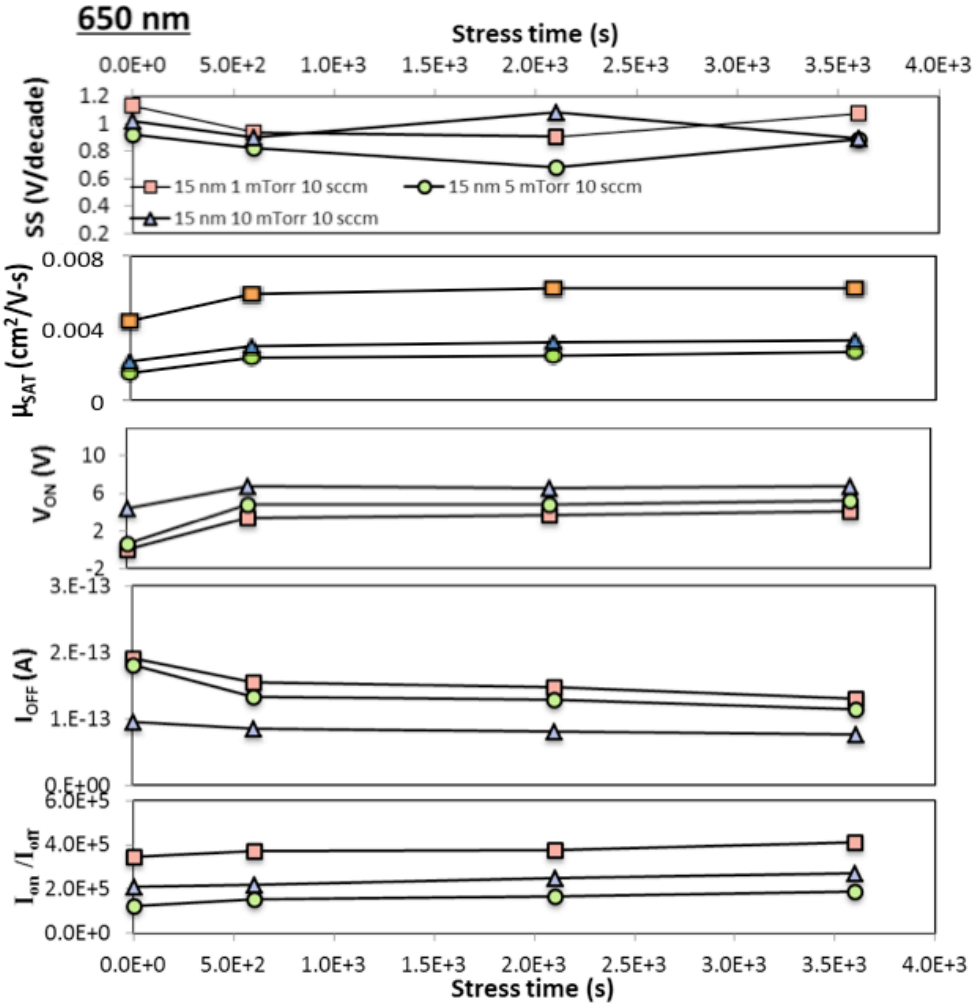

Figure 33. The influence of wavelength 650 nm on 140°C annealed GSZO TFTs.

As shown in Figure 33. unlike literature, the illumination of red light on 140°C annealed GSZO TFTs caused a positive V_{ON} shift (~4.2 V) within 10 mins for the 1 and 5 mTorr device, but becomes stable thereafter. The 10 mtorr exhibited a smaller V_{ON} shift (2.4 V). Since a

positive shift in V_{ON} constitutes a net decrease in electrons within the film it is believed that more charges are being trapped than generated and after 10 minutes a stable balance where the rate of charges trapped equals the rate of charges generated. The 10 mTorr device is shown to have the smallest ΔV_{ON} suggesting the total density of shallow traps is lower than that of the 1 mTorr and 5 mTorr devices. I_{OFF} is invariant for all devices, which is expected since a large increase in carrier concentration is not observed for all samples.

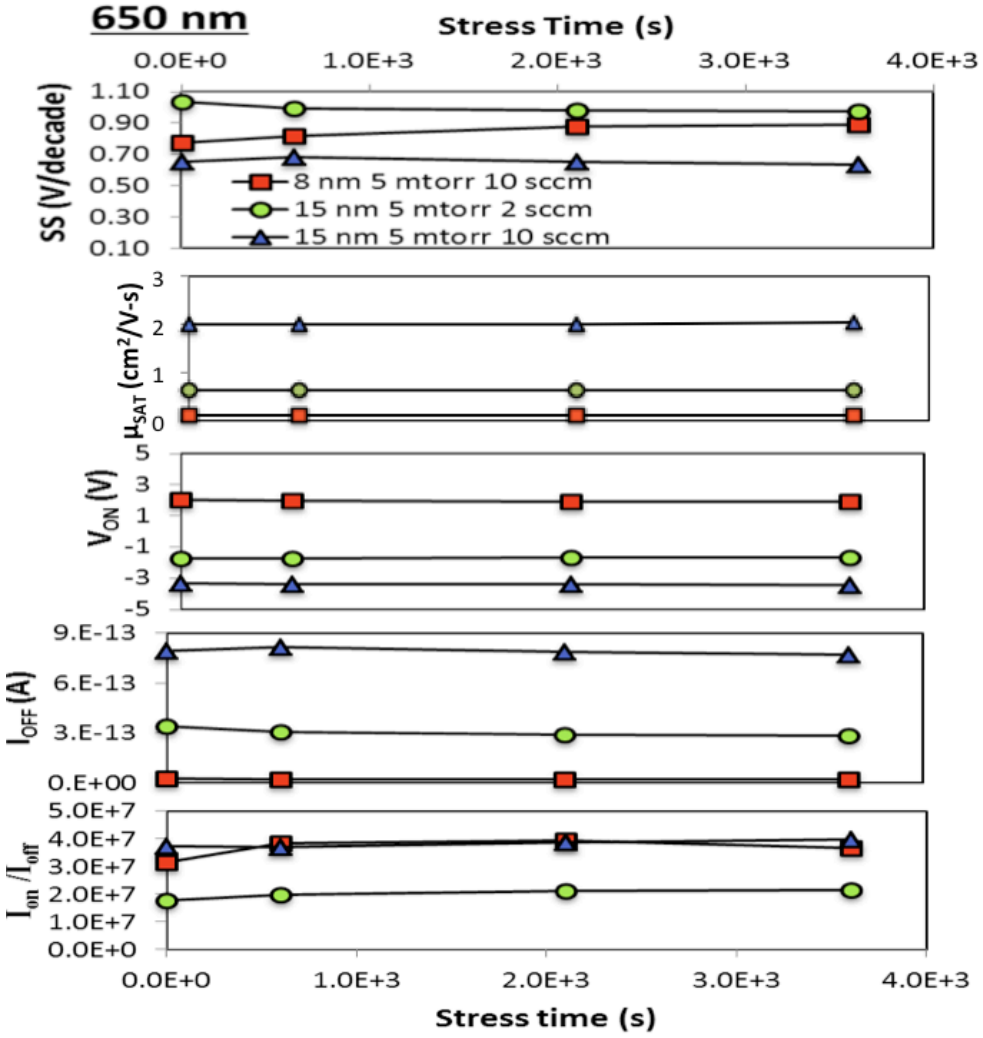

Figure 34. The influence of wavelength 650 nm on 450°C annealed GSZO TFTs.

As shown in Figure 34. similar to literature, the illumination of red light on 450°C annealed GSZO TFTs results in little to no V_{ON} shift in the transfer characteristics. The shift is

extremely small and 10 sccm devices ($\Delta V_{ON} \sim 0.14$ V) seem to exhibit somewhat higher V_{ON} shift with respect to 2 sccm ($\Delta V_{ON} \sim 0.07$ V). High temperature devices are very stable at this wavelength, indicating significant reduction in the shallow traps.

The 550 nm light has photon energy of ~2.3 eV, which excites electrons trapped in the CB tail states, shallow traps, mid traps as well as lower-energy deep traps as shown in Figure. 32b.

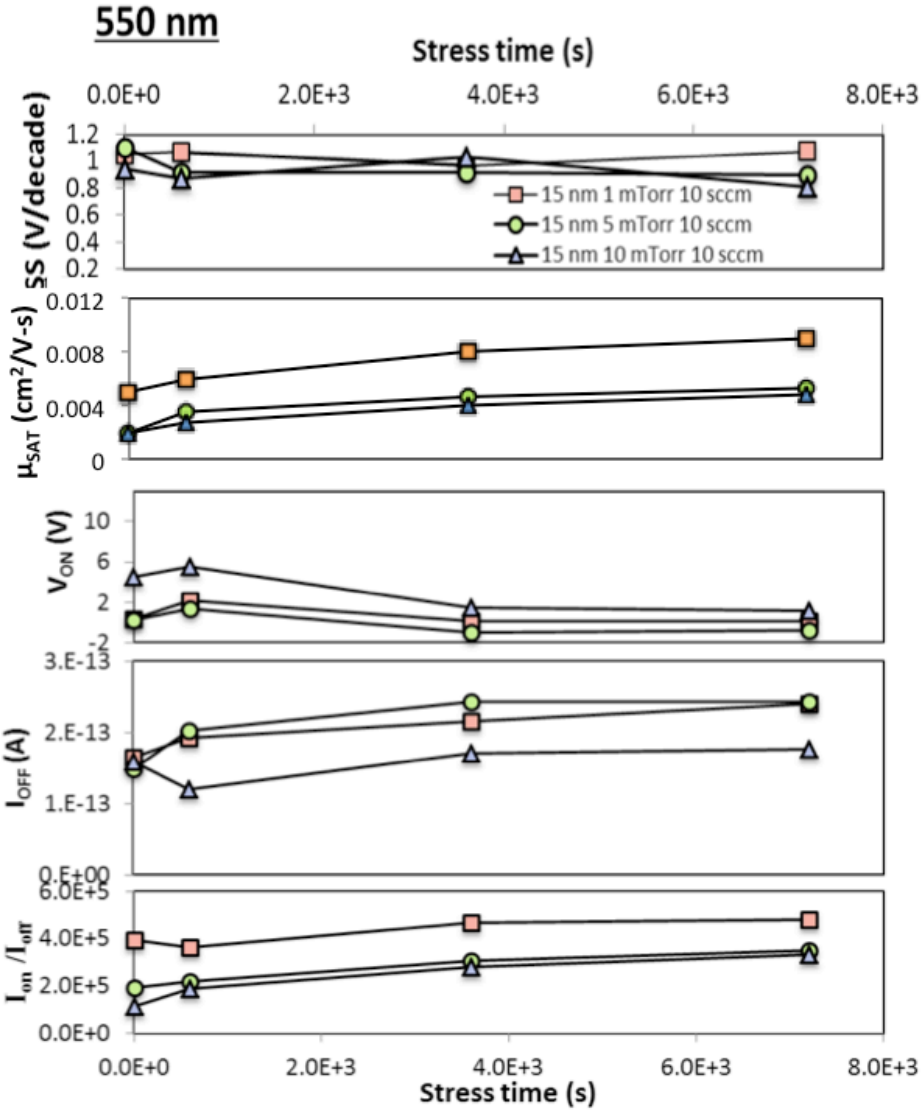

Figure 35. The influence of wavelength 550 nm on 140°C annealed deposition GSZO TFTs.

As shown in Figure 35. unlike literature [20], the illumination of green light (550 nm) on 140°C annealed GSZO TFTs caused a positive V_{ON} shift within 10 mins. However, these devices gradually shift negatively thereafter, but the ΔV_{ON} remained stable after 1 hour. This is attributed to the following process: 1) the charges being trapped outnumber the photo-generated charges within the first 10 mins, and 2) the trap states being filled and the photo-generated charges increases the carrier concentration and shifts V_{ON} negatively. The 1 mtorr device has the largest initial positive shift and then return to its original state with no significant change in SS indicating a low density of deep traps. However, the 5 and 10 mtorr continuously shift negative afterwards. The 10 mTorr device showed the largest negative V_{ON} shift of ~5 V. I_{OFF} remained invariant while SS slightly degraded for the 5 mTorr and 10 mTorr devices. This suggests the 10 mTorr device has a large density of deep traps.

It is well known that deep traps in ZnO films mainly consist of neutral V_O's which requires ~2.3 eV to excite 2 electrons into the CBM resulting in interface trap density, D_{it}, a shallow level close to the conduction band associated with V_O^{2+} [40]. This is also consistent with the changes in SS observed only in the 5 mTorr and 10 mTorr devices indicative of increased D_{it} and the dominance of V_O transition. The 1 mTorr is most stable as it returns to its initial performance after 1 hour and remains.

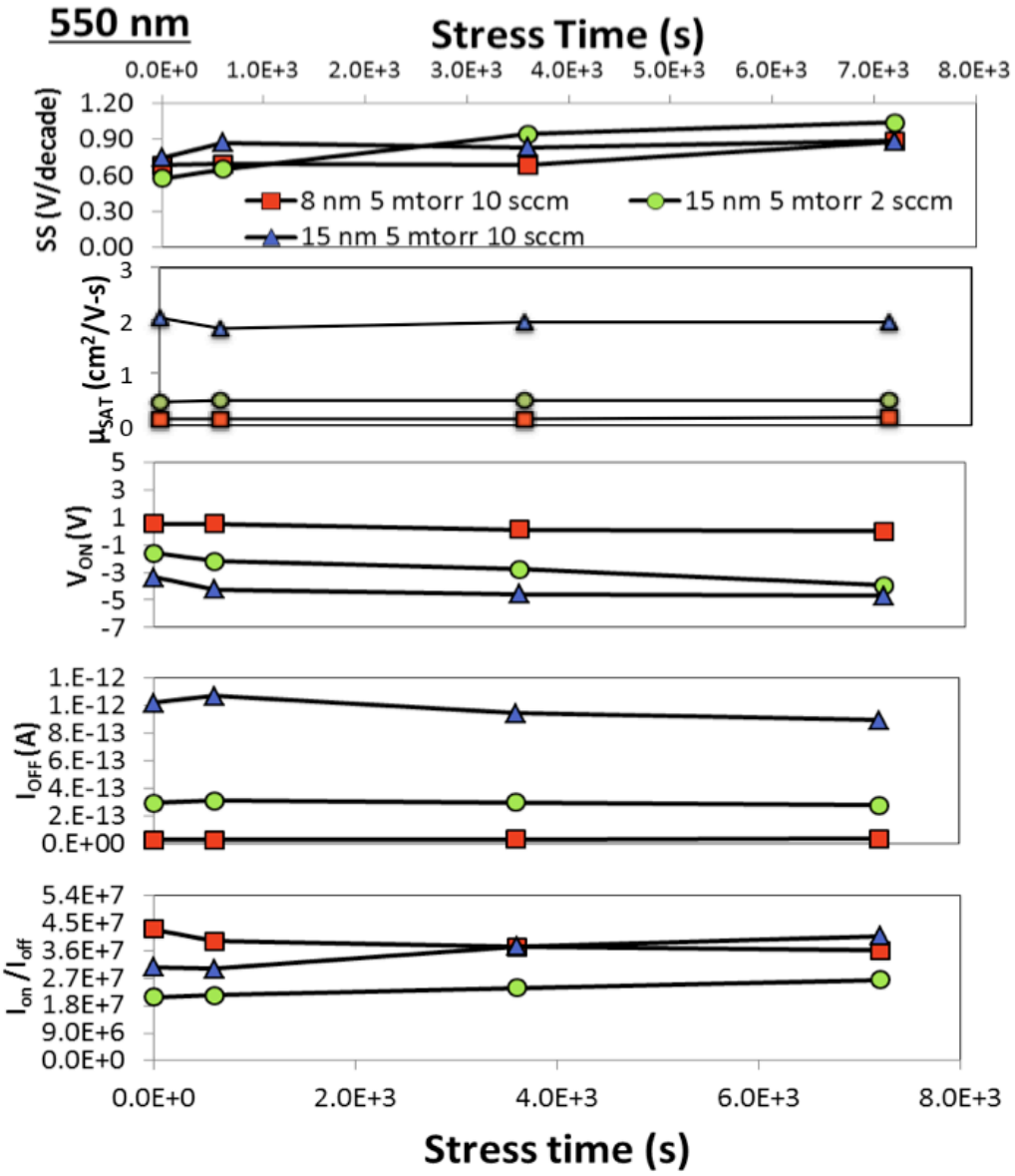

Figure 36. The influence of wavelength 550 nm on 450°C annealed deposition GSZO TFTs.

The effect of green light illumination on 450°C annealed GSZO TFTs is very small. As observed in Figure. 36, there was no significant degradation for 450°C annealed TFTs under this condition .The V_{ON} shifts negatively, and the magnitude for ΔV_{ON} is larger for the 2 sccm sample. The SS is observed to increase with thicker channel, indicating a small increase in D_{it} due to photo-ionization of deep traps occurring. The thinner channel devices show the best

stability with very little change in the characteristics. Most degradation in 2 sccm was due to the presence of more oxygen vacancies in this device contributing to higher background carrier concentration on illumination.

The 410 nm light has photon energy of ~3.0 eV which is in the vicinity of the valence band tail states as shown in Figure. 32b.

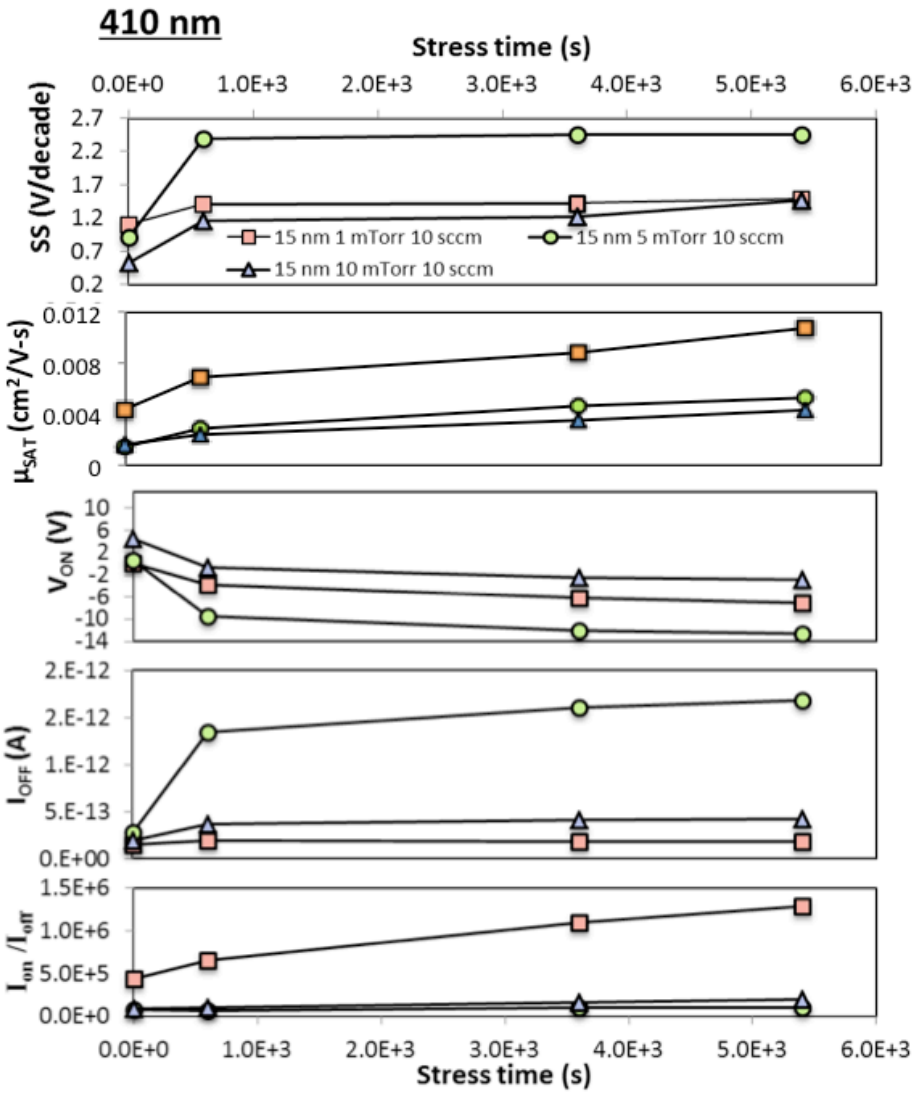

Figure 37. The influence of wavelength 410 nm on 140°C annealed deposition GSZO TFTs.

As shown in Figure 37., the most notable changes in 140°C annealed devices are induced by the near ultraviolet illumination due to increases carrier concentration in the channel region: V_{ON} shifts negatively, I_{OFF} increases, and SS degrades. This is attributed to ionization of oxygen vacancies from V_O to V_O^{2+}, and carriers being excited from the valence band tail states. The 5 mTorr device exhibited the most changes (ΔV_{ON} = -12 V, ΔSS =1.54 V, ΔI_{OFF} =1 order of magnitude) indicating that is has the highest density of VB tail states. Both the 1 mTorr and 10 mTorr devices show similar ΔV_{ON}, I_{OFF} and SS degradation, suggesting the total density of traps within the band gap of these films are nearly the same however distributed differently. Since XRR data shows the 1 mTorr film to be most porous, AFM data shows it to be most rough, and XPS data reveal high hydroxyl contaminants even 5 nm below the surface [9], this somewhat lower shift in V_{ON} as compared to 550 nm could be due to the presence of large density of shallow traps and the carriers generated by 410 nm can also be trapped in these sites giving rise to positive V_{ON} and overall resulting in less shift.

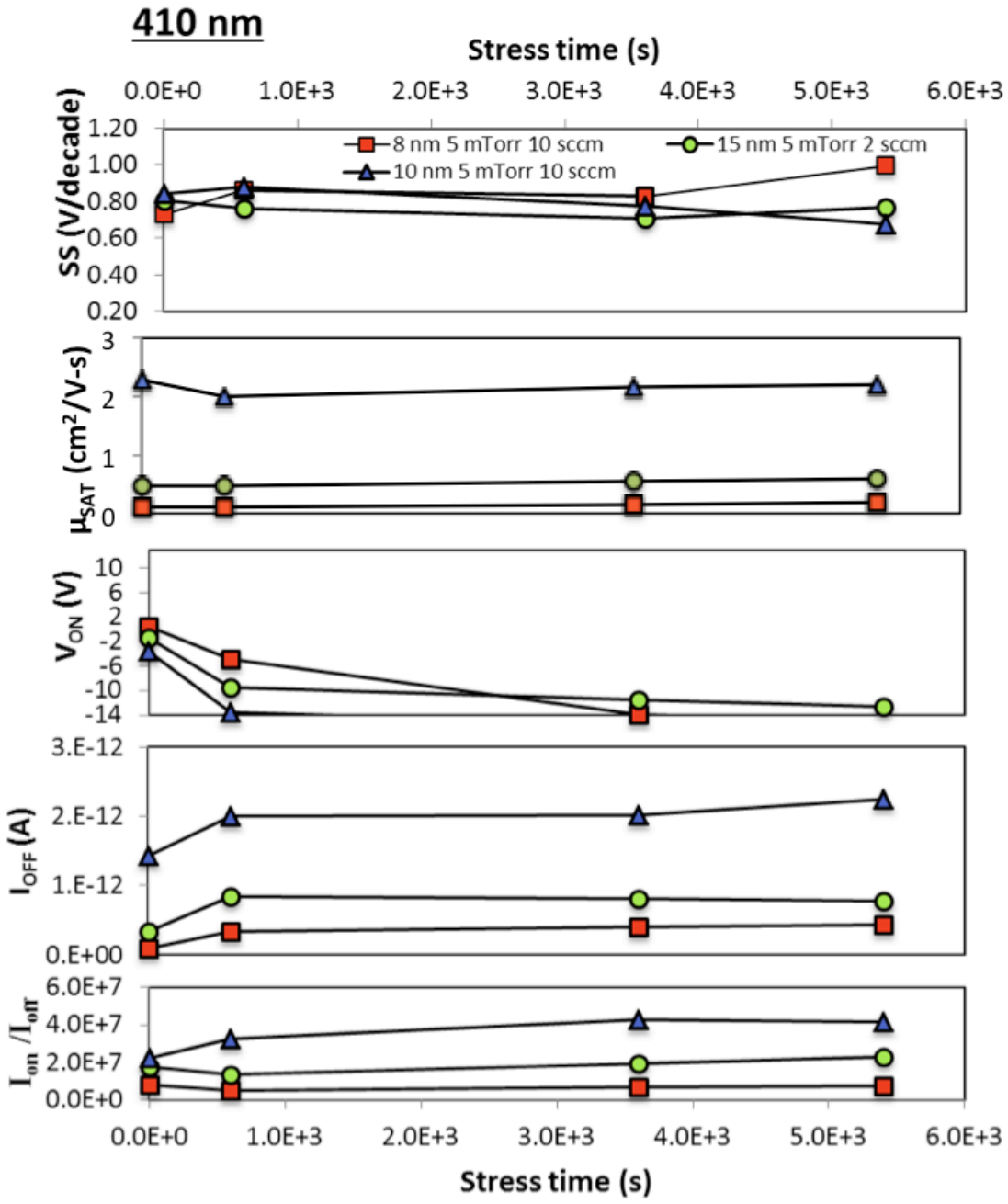

Figure 38. The influence of wavelength 410 nm on 450°C annealed GSZO TFTs.

Most notable changes are induced by the near ultraviolet illumination even in the case of 450°C annealed GSZO devices, as shown in Figure 38. There was a significant negative shift in V_{ON} due to an increased carrier concentration in the channel region. The shift is the largest for thinner channel accompanied with the largest change in SS and I_{OFF} increasing. Since there was

not a significant change observed for 550 nm, it is indicative of the fact that these changes are not due to deep traps but due to valence band tail state, which has a much large density. The increase in I_{OFF} is also consistent with this fact. The thicker channel devices were more stable. The 450°C annealed devices show a less change in V_{ON} and also less change in SS indicating that the devices are more dominated by deep traps rather than the tail states as it also shows a significant changes at 550 nm.

4.3.3 Instability of negative bias illumination stress. The transfer characteristics of GSZO TFTs exposed to a wavelength of 550 nm with a bias of -15 V for 2 hrs., were seriously degraded when a DC negative bias stress was applied in the existence of light illumination, as shown in Figure 39.

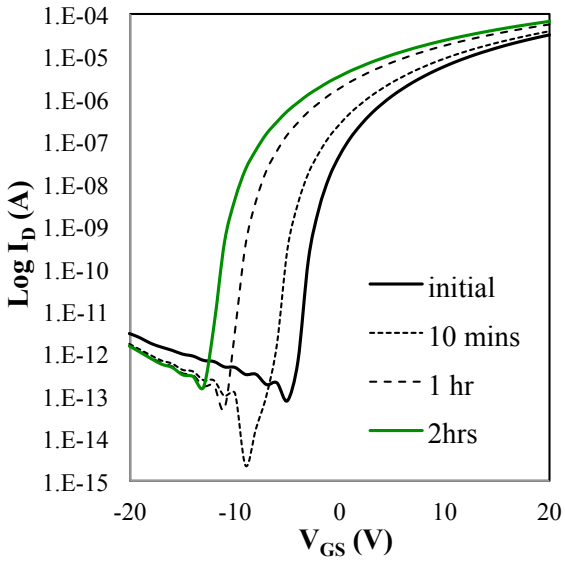

Figure 39. Typical transfer characteristics of GSZO under a negative bias (-15 V) illumination stress (λ = 550 nm).

4.3.3.1 Low temperature annealed GSZO TFTs. As observed in Figure 40., the application of NBIS induces instability on the figure of merits for all devices: SS degrades

instantly (< 10 mins); V_{ON} shifted negatively; μ_{SAT}, I_{OFF} and I_{ON}/I_{OFF} decreases for all devices. The sample at higher pressure exhibited the most degradation during this stress condition.

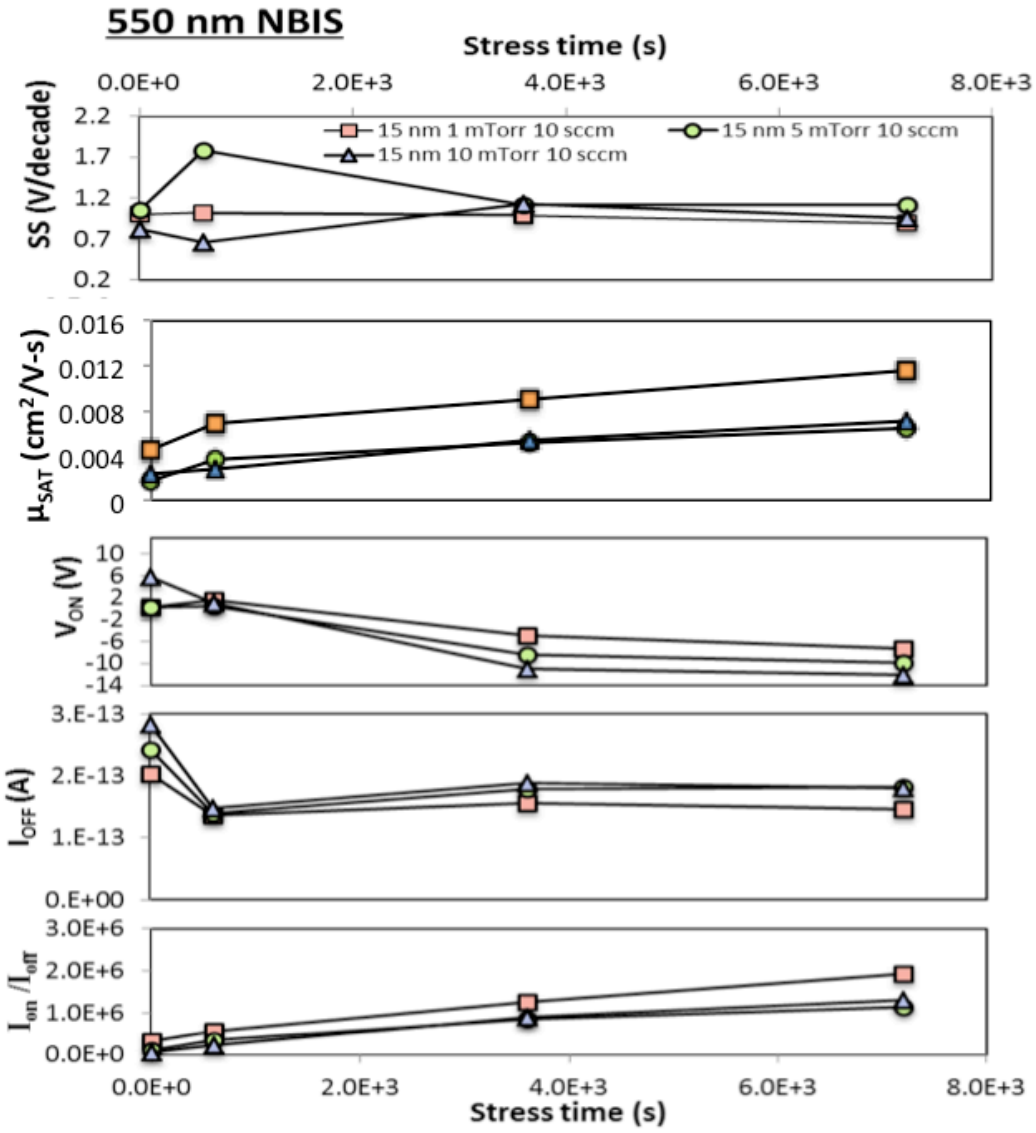

Figure 40. The influence of NBIS on 140°C annealed GSZO TFTs.

The 1 mTorr device showed a positive shift in V_{ON} while V_{ON} the 5 mTorr device remained invariant and shifted negatively for the 10 mTorr device. Thus after 10 minutes a net decrease in carrier concentration exists in the 1 mTorr device due to the large density of shallow traps in the film. The 5 mTorr device showed no change in V_{ON} due to the balance of charge-hole

creation and charge trapping. A decrease in shallow traps exists for the 10 mTorr devices, which explain the negative shift in V_{ON} due to the net increase in carrier concentration. After 10 minutes V_{ON} shifted negatively (~6 V) for the 1 mTorr device with NBIS as opposed to 550 nm illumination with no bias. The negative bias applied to the gate allowed the migration of V_O traps to the semiconductor/gate oxide interface which subsequently trapped hole carriers generated through photo-absorption thus further increasing the electron concentration in the film . Both the 5 and 10 mTorr devices also exhibited a negative V_{ON} shift however the 10 mTorr device exhibited a much larger negative shift. Since the 550 nm wavelength light does not excite carriers from the VB tail states, the 10 mTorr showed the larger V_{ON} shift since the wavelength dependence measurements showed the 10 mTorr device to have the highest density of deep traps. Though SS degraded due to the increase in carrier concentration for all devices, I_{OFF} remained roughly invariant due to the smaller energy wavelength light. Thus the 10 mTorr device showed to be most unstable after NBIS experiments with 550 nm light due to large density of deep traps.

4.3.3.2 High temperature annealed GSZO TFTs. As observed in Figure 41., minor degradation was shown in these devices: no significant change in SS; V_{ON} shifted negatively; I_{OFF} decreased within 10 mins. However the thinner sample (8 nm 5 mtorr 10 sccm) was the most stable of them all, with only a minor degradation in all the characteristics.. This is clear indicative of significant reduction in all the traps including the interface traps in the thinner channel. The XRR data though on low temperature annealed films seem to indicate smoother roughness for thinner channel, which also may impact on the reduced trap density. The 2 sccm has the largest shift thus largest density of traps.

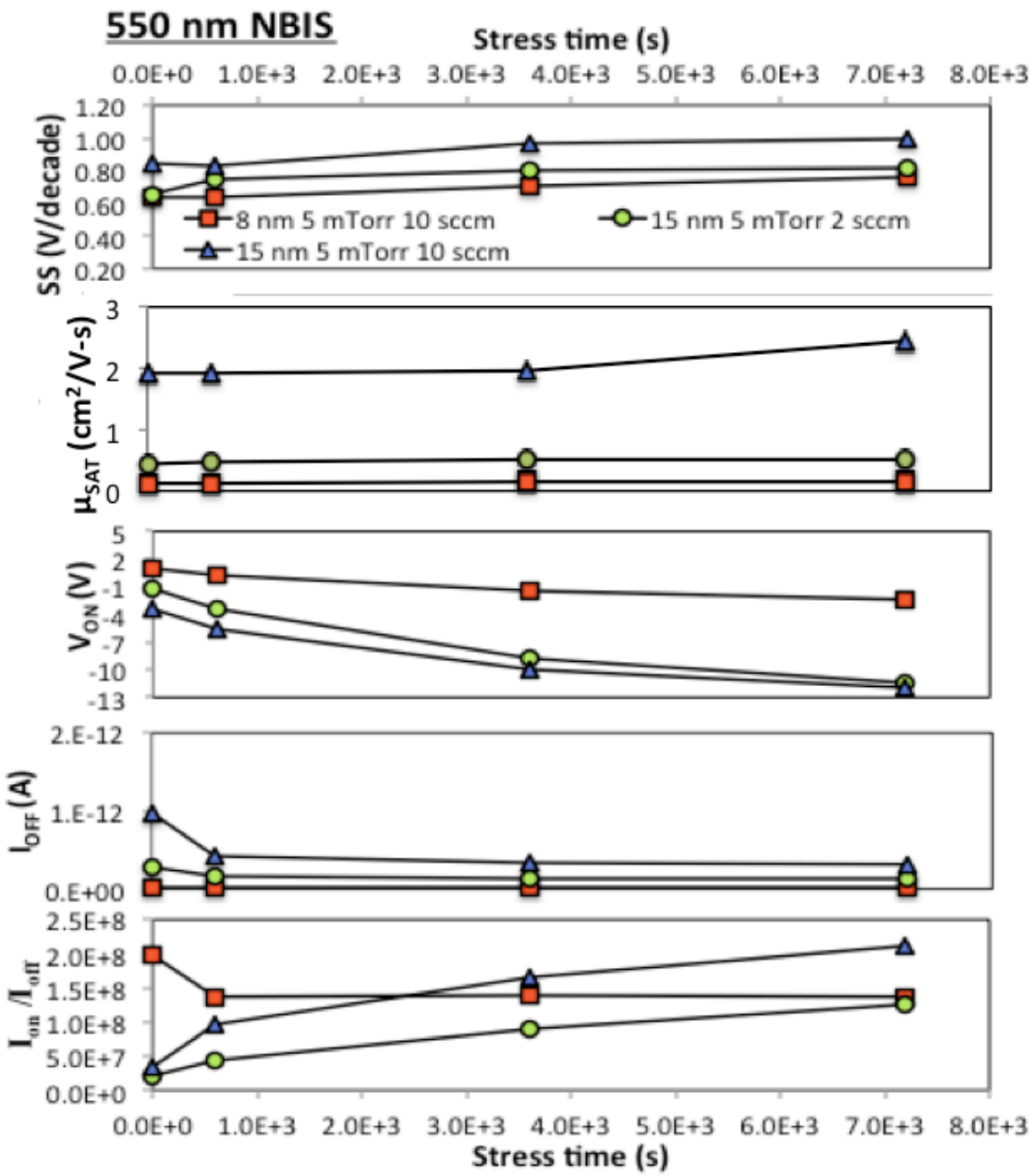

Figure 41. The influence of NBIS on 450°C annealed GSZO TFTs.

4.3.3 Instability of positive bias illumination stress. The transfer characteristics of GSZO TFTs exposed to a wavelength of 550 nm with a bias of +15 V for 2 hrs., were seriously degraded when a DC positive bias stress was applied in the existence of light illumination, as shown in Figure 42.

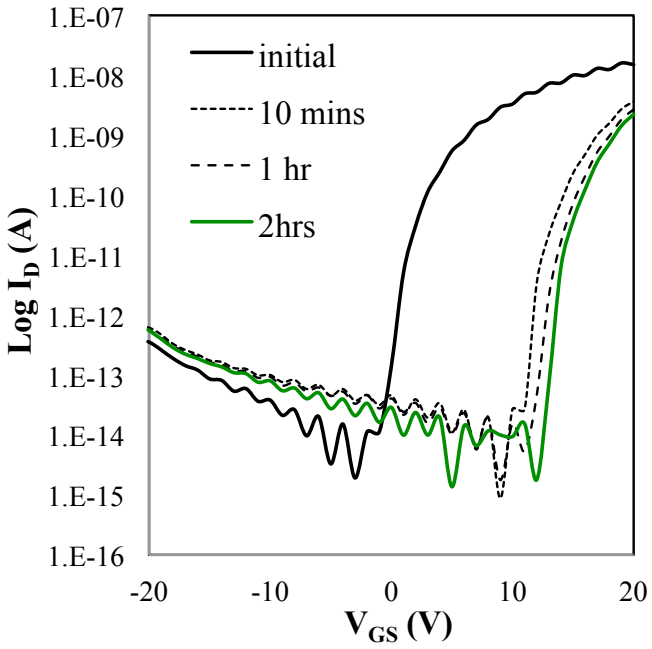

Figure 42. Typical transfer characteristics of GSZO under a positive bias (+15 V) illumination stress (λ = 550 nm).

Under PBIS all the low temperature annealed devices exhibits a positive shift, which is due to the trapped carriers exceeding the photogenerated carriers. The dominance of trap over the free carrier generation is due to low illumination intensity used. A small hump was observed in the 1 mTorr further indicates that Z_{ni}^{2+} density is much more than the free carrier generation. A slight hump is also observed in other samples indicative of the presence of Zni though probably of smaller density.

4.3.4 Effect of illumination stress on CV. To investigate the interface characteristics in detail, the response of GSZO TFTs to three critical wavelengths were verified using C-V measurements. The evolution of C-V curves of different 140°C and 450°C annealed GSZO TFTs as a function of wavelength is shown in Figure 43 -44, respectively.

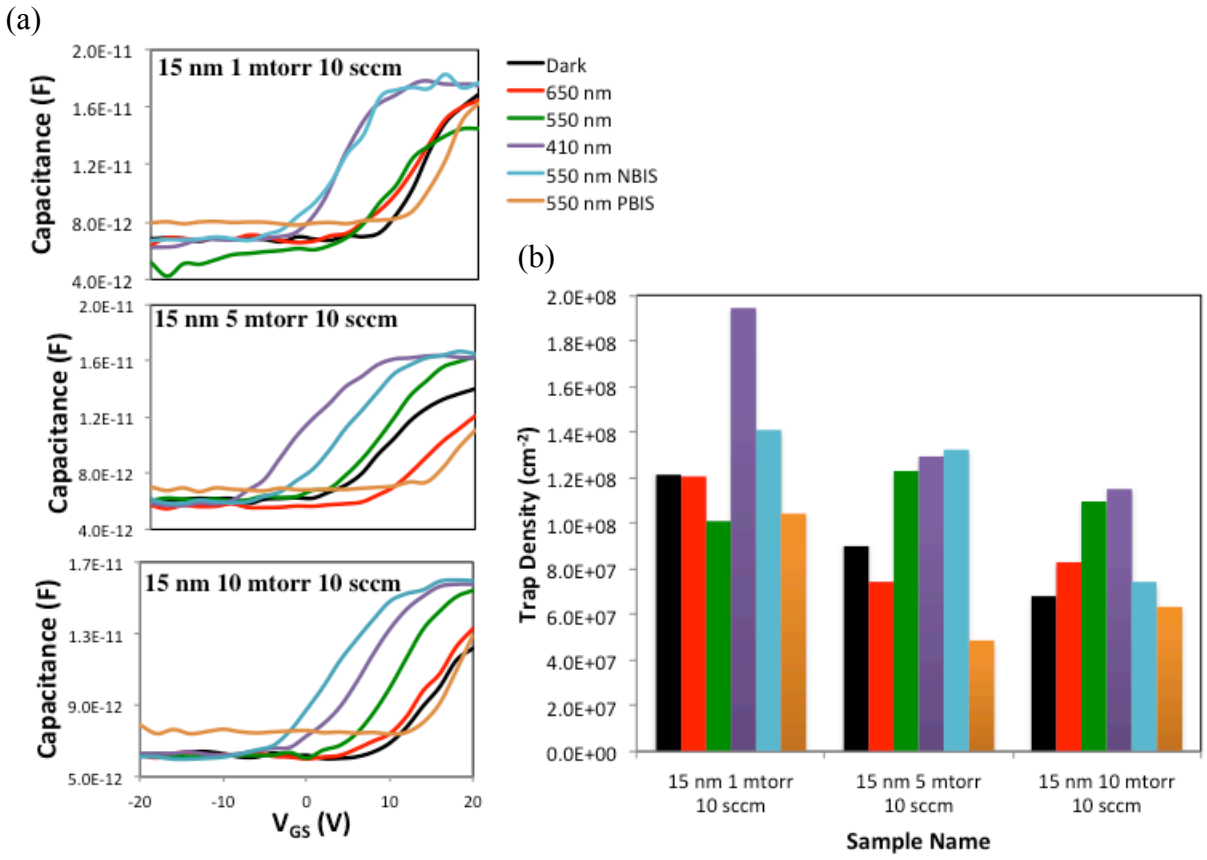

Figure 43. The (a) C-V measurements of 140°C annealed GSZO TFTS and (b) the calculated trap density of each sample under different wavelength illumination.

C-V measurements show a larger capacitance for the 1 mTorr device than the 5 mTorr and 10 mTorr devices most likely due to the large channel conductivity in the 1 mTorr. There was a gradual increase in V_{FB} with increasing deposition pressure consistent with the I-V measurements. The slope of the 10 mTorr device is shown to be higher than the 1 mTorr and 5 mTorr devices indicating a lower concentration of traps excited at 650 nm wavelength. The 5 mtorr device had the largest shift and thus the highest density of occupied trap sites. At 550, the C-V data is also consistent in that the 1 mTorr device shows the lower C_{acc} as compared to the other devices indicative of the large presence of electron traps.

Based on all the above data it appears the 10 mTorr devices have the highest density of deep traps and largest number of V_O to V_O^{2+} transitions. At 410 nm, the measurements show the

5 mTorr device to have a V_{FB} in the negative region and a small slope between the depletion and accumulation regions. These measurements also show the 1 mTorr device to have a larger capacitance with a fully formed accumulation region suggesting it has a higher carrier concentration than the 10 mTorr device, which can be clearly seen from the I-V data.

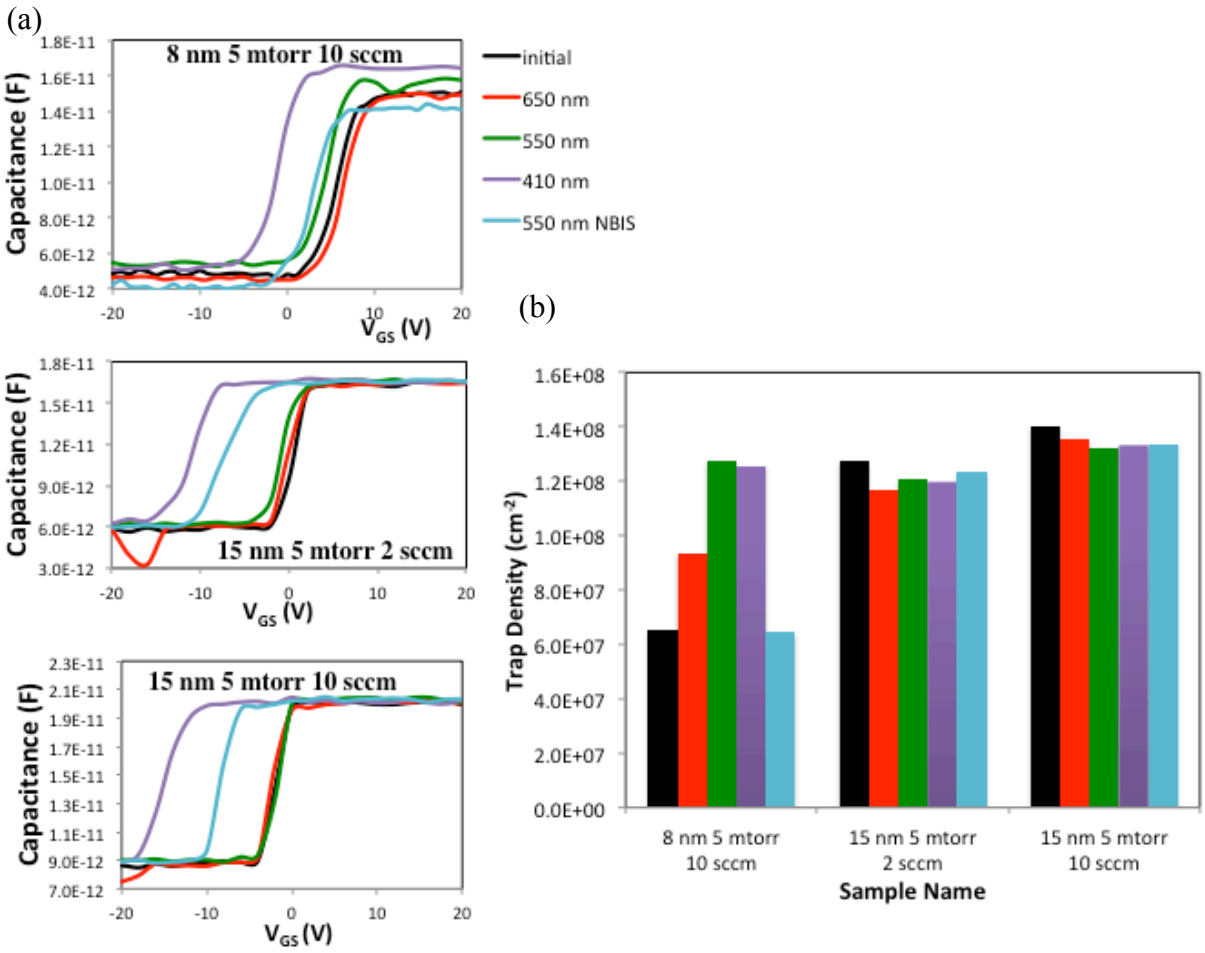

Figure 44. The (a) C-V measurements of 450°C annealed GSZO TFTS and (b) the calculated trap density of each sample under different wavelength illumination.

For all devices, there was a parallel shift in the C-V curve with decreasing wavelength. For low temperature annealed devices, the number of trap states in GSZO TFT increased with decreasing wavelength, indicating that the amount of charge stored is sensitive to the wavelength. However at 650 nm, there was a small positive shift for the thinner channel that was not observed in

thicker channel devices, which was due to photo-induced electron interface traps being generated. However, this change was not noticeable in the I-V characteristics of the thinner sample. At 550 nm, the C_{acc} is increased due to the increase in carrier concentration in the channel, which in turn indicates that the effect of traps is comparatively small with respect to the 10 sccm devices. For the thinner channel device, there is a change in capacitance, which is indicative of change in shallow trap density and speculated to be reduction in the trap density under illumination, which improved C_{acc}. However, for the thicker channels devices, the trap density did not change. This clearly indicates that as the channel layer becomes thin, the surface affects significantly the interface traps and any modification of the surface is impacted in the transfer characteristics. For high temperature deposition conditions, the number of trap states slightly changed, indicating that annealing improves the stability of GSZO TFTs.

To clarify the mechanism of the degradation of the illumination stress and NBIS, the energy band diagram during the stress is shown in Figure 45. As forementioned, the energy band at initial state is assumed to be at flat-band as shown in Figure 45 a. When applying an illumination stress onto the device, two kinds of major degradation behaviors are observed: 1) parallel shift of the transfer characteristics in the negative direction and 2) a hump in the subthreshold region. When an illumination of 550 nm is applied to the device, the neutral V_O in the lower energy band below the Fermi level E_F is either ionized into V_O^+ or Vo^{+2} by absorbing the photon energy and emitting electrons. If the photon energy is not high enough, such as for λ=650 nm, then this process does not occur. When the NBIS is applied, the E_F is lowered as result of accumulation of the positive charges caused by the capture of holes from the valence band either due to the neutral or singly ionized oxygen vacancies.

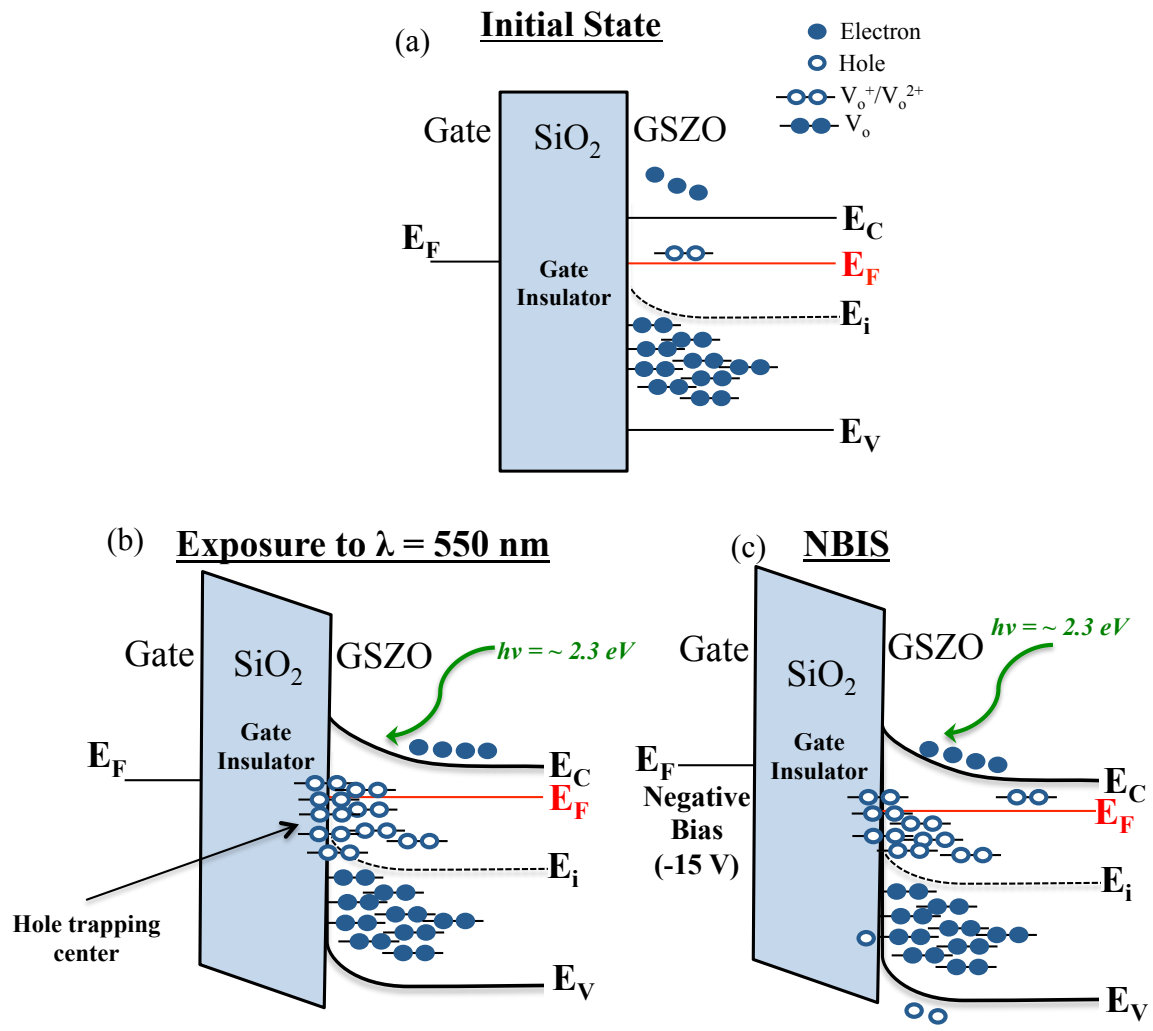

Figure 45. Energy band diagram of the GSZO TFT (a) at initial state, under (b) illumination stress (550 nm), and (c) NBIS.

The trap density ,D_{it}, observed near the CB edge in GSZO TFTs can possibly be related to the doubly ionized oxygen vacancies (V_o^{2+}), according to literature [51, 52]. The neutral oxygen vacancies (V_o) is relaxed to form a fully occupied deep state near the valance band, which no longer traps an electron and is inactive for electron transport [40, 53]. However, under the light illumination of $\lambda \leq 550$ nm, the electrons from V_o can be photo-excited to the conduction band, thus resulting in an increase in I_{OFF} and defect transition to V_o^{2+}. Therefore, the

increase in trap density is attributed to defects levels generated by V_o^{2+} under light illumination at $\lambda \leq 550$nm. This can possibly induce an increase in SS in the transfer curves as observed.

4.4 Shelf Life Stability

It was observed that thin films could degrade after being exposed to room air for several weeks. Figure 13 shows how varying annealing time affects the amount of shift in V_{ON} over a period of 11 weeks. Although the 12 hr sample had poorer shelf life stability, V_{ON} for both the devices tend to merge after 2 weeks and remained stable after that. A possible explanation of this behavior could be hydrolyzation by air moisture.

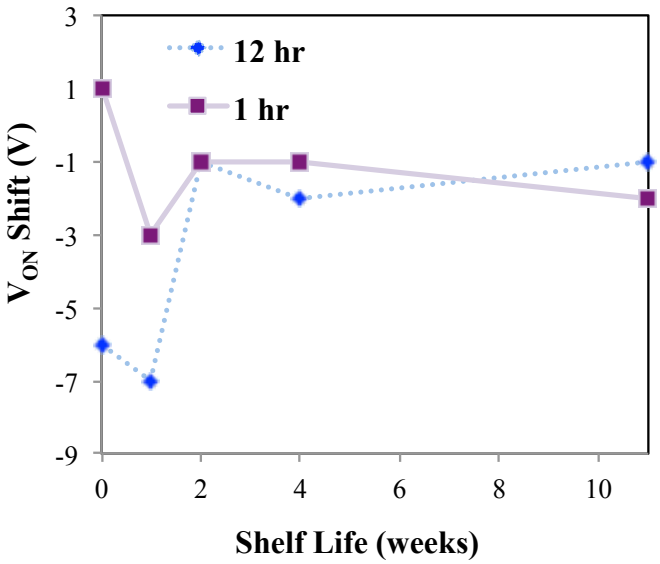

Figure 46. V_{ON} shift as a function of shelf life for GSZO TFTs which employ different annealing duration: 1hr and 12hr at 140 °C post deposition.

4.5 AIM-Spice Simulated Results

A physical I-V model based on the exponential density of deep and tail states has been developed and tested for modeling GSZO TFTs. The accuracy of the simulated curves using the parameters extracted is verified with measured and calculated data using the expressions contained in the Si:H TFT model level 15.

Table 11

Parameters used to model the GSZO TFTs

Name	Units	Default
ALPHASAT	-	0.6
CGDO	F/m	0
CGSO	F/m	0
DEF0	eV	0.6
DELTA	-	5
EL	eV	0.35
EMU	eV	0.06
EPS	-	11
EPSI	-	7.4
GAMMA	-	0.4
GMIN	$m^{-3}eV^{-1}$	1.0×10^{23}
IOL	A	3.0×10^{-14}
KASAT	1/°C	0.006
KVT	V/°C	-0.036
LAMBDA	1/V	0.0008
M	-	2.5
MUBAND	m^2/V-s	0.001
RD	Ω	0
RS	Ω	0
SIGMA0	A	1.0×10^{-14}
TNOM	°C	27
TOX	m	1.0×10^{-7}
V0	V	0.12
VAA	V	7.5×10^{3}
VDSL	V	7
VFB	V	-3
VGSL	V	7
VMIN	V	0.3
VTO	V	0

The linear characteristics calculated were compared with the experimental data and the simulated using AIM-SPICE. Both simulated and calculated are practically the same and fit well with the experimental data, validating the proposed new extraction method as shown in Figure 47.

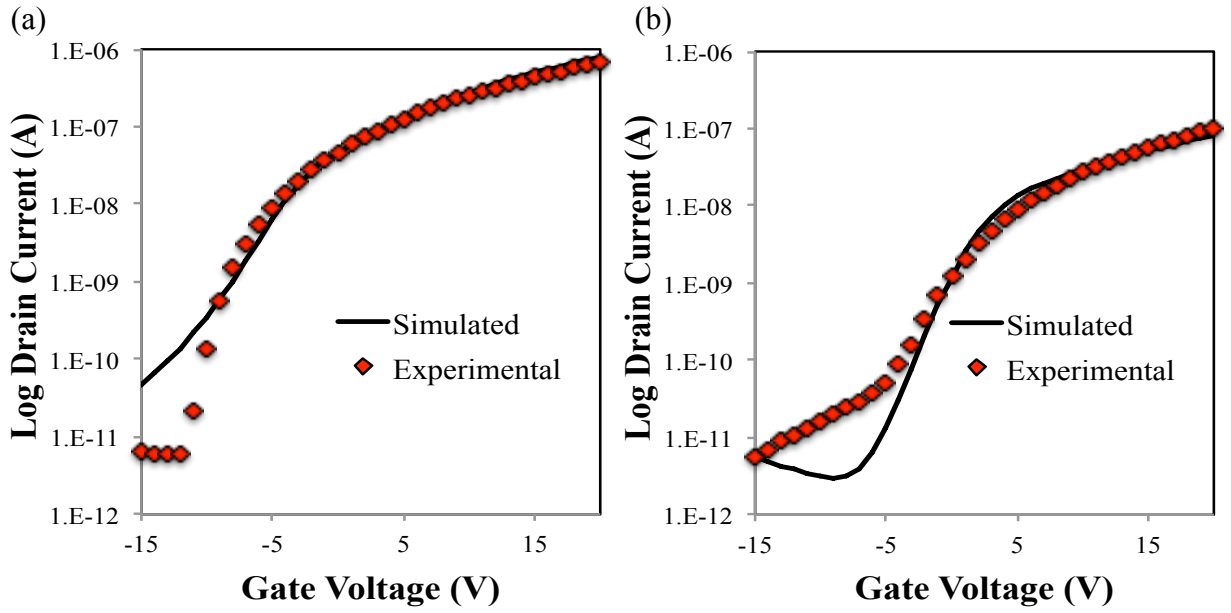

Figure 47. Comparison between simulation and measured data for devices with (a) W/L=100/50 and (b) 75/25 on a semi-log scale.

Some limitation of this software is that it could not fit the simulated data to the measured data in the region below V_{ON}. The extracted parameters varied per device, as shown in Table 7.

Table 12

Extracted parameters from AIM-Spice

Sample	Gamma	Delta	Gmin ($m^{-3}eV^{-1}$)	Vmin (V)	Vaa (V)	Muband (m^2/V-s)
400°C 5 mTorr 10 sccm	1.4	10	1.0×10^{23}	0.7	50	1.28×10^{-4}
350°C 5 mTorr 2 sccm	0.6	4	5.0×10^{20}	0.4	80	2.06×10^{-3}
350°C 5 mTorr 2 sccm	1	10	1.0×10^{23}	0.9	100	2.79×10^{-5}
350°C 5 mTorr 2 sccm	0.85	7	1.0×10^{23}	0.8	40	7.6×10^{-6}
140°C 10 mTorr	0.45	9	1.0×10^{23}	0.3	80	8.0×10^{-6}
140°C 5 mTorr	0.15	7	3.0×10^{23}	0.3	750	4.1×10^{-6}
350°C 5 mTorr	0.55	9	1.0×10^{23}	0.4	550	2.79×10^{-4}

The transfer curve simulated for each device varied in each extracted parameters: gamma, delta, gmin , vmin, vaa, and muband. There, was no trend in these parameters, however, for the gmin (density of trap deep states), the 140°C annealed 5 mtorr sample appeared to have the highest value (3×10^{23} $m^{-3}eV^{-1}$) while the 350°C annealed 5 mtorr had the least (5×10^{20} $m^{-3}eV^{-1}$). This is consistent with XRR analysis and stability measurements discussed earlier. All other variations in the other parameters are due to different fabrication conditions.

CHAPTER 5

Discussion and Future Research

5.1 Discussion

This thesis studied how various processing parameters such as annealing temperature, oxygen atmospheric pressure, and thickness affect the stability of GSZO TFT characteristics. This also provides information on the trap density in the original annealed devices and hence on the performance of the device. Understanding the problem in the electrical and optical stability of TFTs for prolonged time periods is a major performance issue for these devices. There are findings that annealing is effective in reducing bias stress and light-induced instabilities. In this work, the structural, electrical, and optical properties were investigated to understand the origin of instability in GSZO TFTs. The degradation behavior of GSZO TFTs transfer characteristics under a positive and negative stress was also examined. The time dependence of PBS on the electrical characteristics was evaluated. The application of the illumination stress and NBIS plays an essential factor in illustrating the instability using an electron trapping model, and in predicting the locations of the subgap states, which generate light-induced electron-hole pairs.

XRR analysis showed the low temperature annealed samples to be more porous than high temperature annealed devices. The high temperature samples were denser and exhibit smoother interface as inferred from XRR data, leading to improved SS and carrier mobility. This explains the significant degradation observed in lower temperature annealed devices.

The application of PBS and NBS showed that the low temperature annealed devices to be less stable than high temperature devices. During the PBS, the positive shift in V_{ON} is due to carriers being trapped in shallow electron traps. The more porous the device, the more degradation observed, thus indicating a higher concentration of shallow electron traps. This

effect was most observed in low temperature annealed (140°C) devices at low pressures (1 mTorr). This device also shows a hump in its electrical characteristics which has been reported to be the presence of Z_{n_I} that forms a second path of charge flow [9]. The presence of the hump gradually reduces with an increase in deposition pressure; this also agrees with the gradual increase in film density with deposition pressure, as shown in the XRR data. The density of shallow defects decreases with increasing pressure, suggesting that higher pressure deposition leads to significant reduction in the shallow electron traps, resulting in a much more stable GSZO TFT with a ΔV_{ON} of only 0.75 V. With an increase in annealing temperature, the density of the devices was much more dense and both shallow and deep electron traps were reduced further. The annealing will remove some of the weak chemical bonds as well. This resulted in a more stable device with great stability with a ΔV_{ON} of 0.24 V. This is also consistent with the τ and β values extracted from the stretched exponential equation, which showed the high annealed samples to have a shorter time constant than the low annealed samples attesting to the improvement in stability with higher annealing temperature.

During the NBS, the negative shift in V_{ON} is due to the migration of positively charged oxygen vacancy induced by negative free carriers in the channel. Again the high temperature annealed devices proved to be more stable than the low temperature samples. All of the devices maintained good stability under negative bias stress compared to the instability induced by the PBS, which is comparative with literature. Overall, the device performance under the application of PBS and NBS of high temperatures samples was much more stable than low temperature samples. The device degradation was severe for PBS.

It is good to note that the most photo-induced degradation of GSZO TFTs occurs under near ultraviolet illumination (λ< 500nm), due to electron-hole pairs that are created by the photo-

excitation originating from band tail states. The salient difference between the low temperature annealed devices is the influence of light-induced traps: the low temperature annealed devices were affected by shallow traps, deep traps, and valence band tail states, while the degradation in high temperature devices were due to the valence band tail states only.

During the NBIS condition with the illumination wavelength at 550 nm, the negative V_{ON} shift is due to electron-hole pairs in the channel region generated by light and the photo-created hole carriers moving toward the gate dielectric by the NBS and become trapped at the interfacial trap states. NBIS instability was induced on both the low and high temperature annealed device, more in the low temperature annealed devices. Furthermore, the instability in the low temperature annealed devices is attributed to a large amount of point defects including oxygen vacancy in the channel layer as confirmed by XRR results. However, there is improvement in the photo-bias stability at lower pressure deposited device due to the carriers passivating the electron traps. The large degradation observed in the 10 mTorr device is indicative of the presence of large density of deep traps at high pressures. The photo-bias stability of the high temperature annealed device improved with the reduction of channel layer both due to the improvement in the quality of the surface, interfaces as well as the channel leading to overall reduction in the subband gap states. When a PBIS was applied on the low temperature annealed devices, a there was a large positive shift due to the combination of increased background N leading to negative shift in V_{ON}. However, the PBS was more dominant in this case as concluded earlier.

There are few reports on modeling of the current-voltage characteristics of oxide TFTs, however, there is a Level 15 SPICE Si:H model that uses exponential distributions of deep and tail states. This method is applied to the linear and saturation regions for extraction of all the above-threshold parameters. The transfer curves of the devices are well produced by using the

proposed model. Comparison of experimental I_{DS}-V_{GS} and I_{DS}-V_{DS} with calculated transfer curves using model expressions to simulated curves in AIM-SPICE using the extracted parameters shows good match higher values of V_{DS}, thus, validating the proposed procedure over a limited region.

5.2 Future Work

The electrical and optical stability of GSZO thin film transistors produced by a number of different techniques has been provided in this thesis. Recommendations for the future direction of GSZO research include: 1) improve the GSZO film quality through better deposition condition (ex. Increase the pressure for low temperature devices, deposition of two layer at varying pressures) and thinner channel, 2) address the effect of more wavelengths over time to provide a more in-depth study of the transfer characteristics dependence on wavelength, 3) evaluation of the kinetics of recovery mechanism under optical stress would yield information on the nature of the energy levels of the defect states involved as to if the changes are permanent or temporary, 4) to fabricate devices with encapsulation thus eliminating the oxygen and water adsorption effects, and 5) modeling of the devices. As with any kind of research work, a large number of issues still remained unexplored and need future work. Overall, the aim is to fabricate stable GSZO devices for commercially implementation of these materials.

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Appendix

Table A. 1

AIM-SPICE Model Level 15 Si:H.

Name	Description	Units	Default
ALPHASAT	Saturation modulation parameter	-	0.6
CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0
CGSO	Gate-source overlap capacitance per meter channel width	F/m	0
DEF0	Dark Fermi level position	eV	0.6
DELTA	Transition width parameter	-	5
EL	Activation energy of the hole leakage current	eV	0.35
EMU	Field effect mobility activation energy	eV	0.06
EPS	Relative dielectric constant of substrate	-	11
EPSI	Relative dielectric constant of gate insulator	-	7.4
GAMMA	Power law mobility parameter	-	0.4
GMIN	Minimum density of deep states	$m^{-3}eV^{-1}$	1.0×10^{23}
IOL	Zero bias leakage current	A	3.0×10^{-14}
KASAT	Temperature coefficient of ALPHASAT	1/°C	0.006
KVT	Threshold voltage temperature coefficient	V/°C	-0.036
LAMBDA	Output conductance parameter	1/V	0.0008
M	Knee shape parameter	-	2.5
MUBAND	Conduction band mobility	m^2/Vs	0.001
RD	Drain resistance	Ω	0
RS	Source resistance	Ω	0
SIGMA0	Minimum leakage current parameter	A	1.0×10^{-14}
TNOM	Parameter measurement temperature	°C	27
TOX	Thin-oxide thickness	m	1.0×10^{-7}
V0	Characteristic voltage for deep states	V	0.12
VAA	Characteristic voltage for field effect mobility (determined by tail states)	V	7.5×10^{3}
VDSL	Hole leakage current drain voltage parameter	V	7
VFB	Flat band voltage	V	-3
VGSL	Hole leakage current gate voltage parameter	V	7
VMIN	Convergence parameter	V	0.3
VTO	Zero bias threshold voltage	V	0

Table A.2

Aim-SPICE extracted parameters

Sample	Gamma	Delta	Gmin ($m^{-3}eV^{-1}$)	Vmin (V)	Vaa (V)	Muband (m^2/Vs)
400°C 5 mTorr 10 sccm	1.4	10	1.0×10^{23}	0.7	50	1.28×10^{-4}
140°C	0.55	13	1.0×10^{23}	0.55	70	1.8×10^{-5}
350°C 5 mTorr 2 sccm	0.6	4	5.0×10^{20}	0.4	80	2.06×10^{-3}
350°C 5 mTorr 2 sccm	1	10	1.0×10^{23}	0.9	100	2.79×10^{-5}
350°C 5 mTorr 2 sccm	0.85	7	1.0×10^{23}	0.8	40	7.6×10^{-6}
140°C 10 mTorr	0.45	9	1.0×10^{23}	0.3	80	8.0×10^{-6}
140°C 5 mTorr	0.15	7	3.0×10^{23}	0.3	750	4.1×10^{-6}
350°C 5 mTorr	0.55	9	1.0×10^{23}	0.4	550	2.79×10^{-4}
140°C Thinner SiO2	0.55	13	1.0×10^{23}	0.75	90	2.27×10^{-5}

Table A.3

XRR Data

Expected Thickness Value	
ZnO	10
ZnO	12.25
ZnO	14.775
ZnO	*15*
ZnO	15.175
ZnO	28.1
ZnO	30
SiO2	123.85
SiO2	100

Sample ID	Thickness		Roughness		Density
	ZnO	SiO2	ZnO	SiO2	ZnO
10mTorr	10.956	121.767	0.5972	0.6412	6.96
20mTorr	6.181	91.905	0.5254	0.1781	6.709
RT	10.502	106.65	0.3939	0.4104	6.636
10nm 5mTorr	9.825	124.442	0.7674	0.4144	6.52
Low ET	9.423	107.1	0.5363	0.5405	6.27
020113 gszo SiO2 Annealed 140	11.321	123.413	0.6483	0.7725	5.961
1mTorr	26.734	120.002	0.3355	0.9243	5.948
15 nm 5mTorr	15.658	122.959	0.5392	0.678	5.881
15 nm 5mTorr 10hr Annealed	13.233	122.056	0.7094	0.522	5.857
3mTorr	25.057	122.217	0.5206	0.7229	5.857
013113 GSzo SiO2 Rt 30nm Annealed 350	28.626	123.057	0.6511	0.9401	5.615
021813 2sccm 15nm 350C Air Ann	15.949	122.996	0.4862	0.6529	5.512
013113 GSzo SiO2 Rt 30nm unAnnealed	28.94	122.798	0.6858	0.9564	5.51
021913 15nm 1mTorr 10sccm	17.752	123.061	0.5692	0.3573	5.43
2sccm 15 nm unAnnealed	16.785	122.606	1.1679	1.0995	5.353
7mTorr	13.084	123.472	0.7782	1.397	5.282
5mTorr	26.868	122.304	1.5751	0.5388	4.581

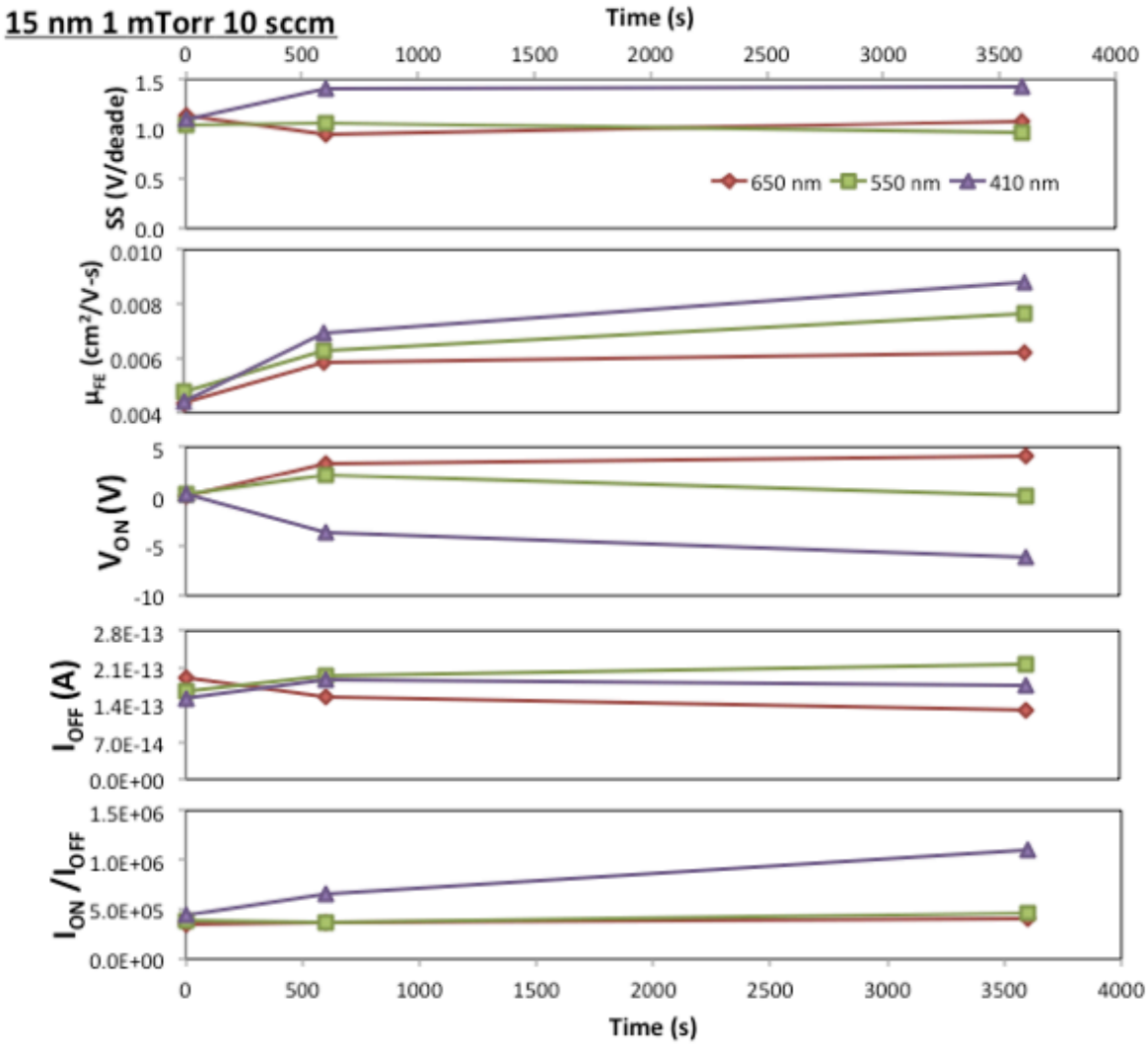

Figure A.1 Low Temperature Deposition Devices

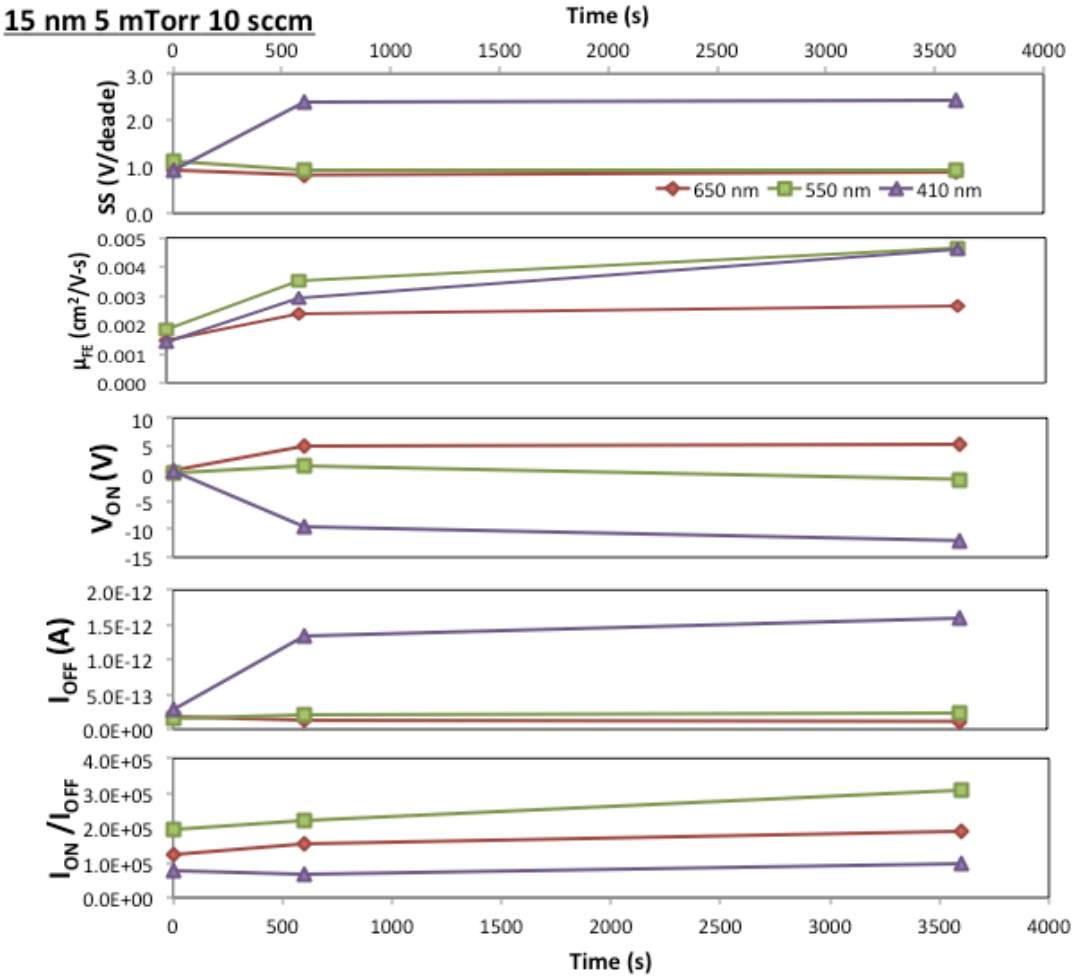

Figure A.2 Low Temperature Deposition Devices

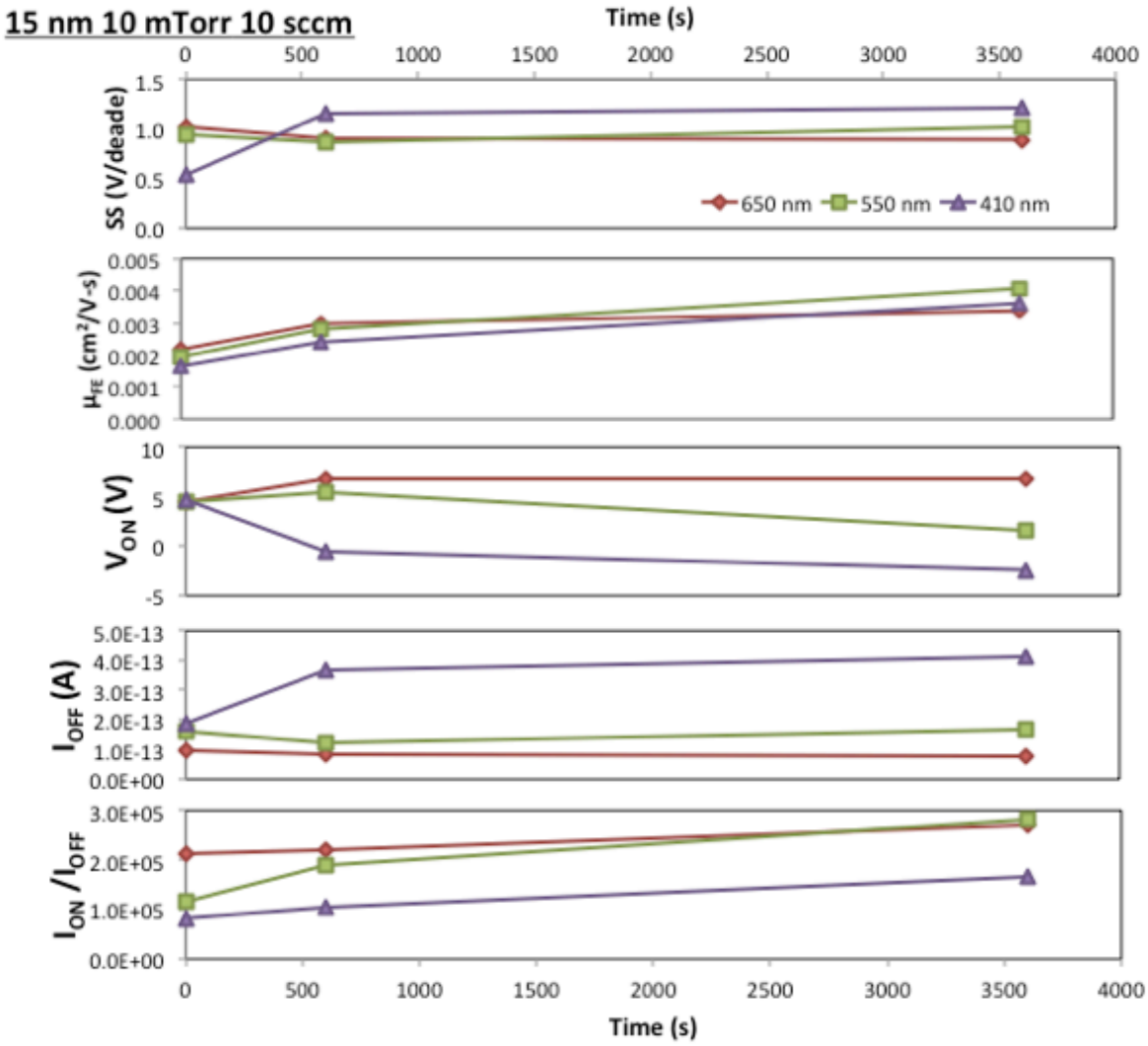

Figure A.3 Low Temperature Deposition Devices

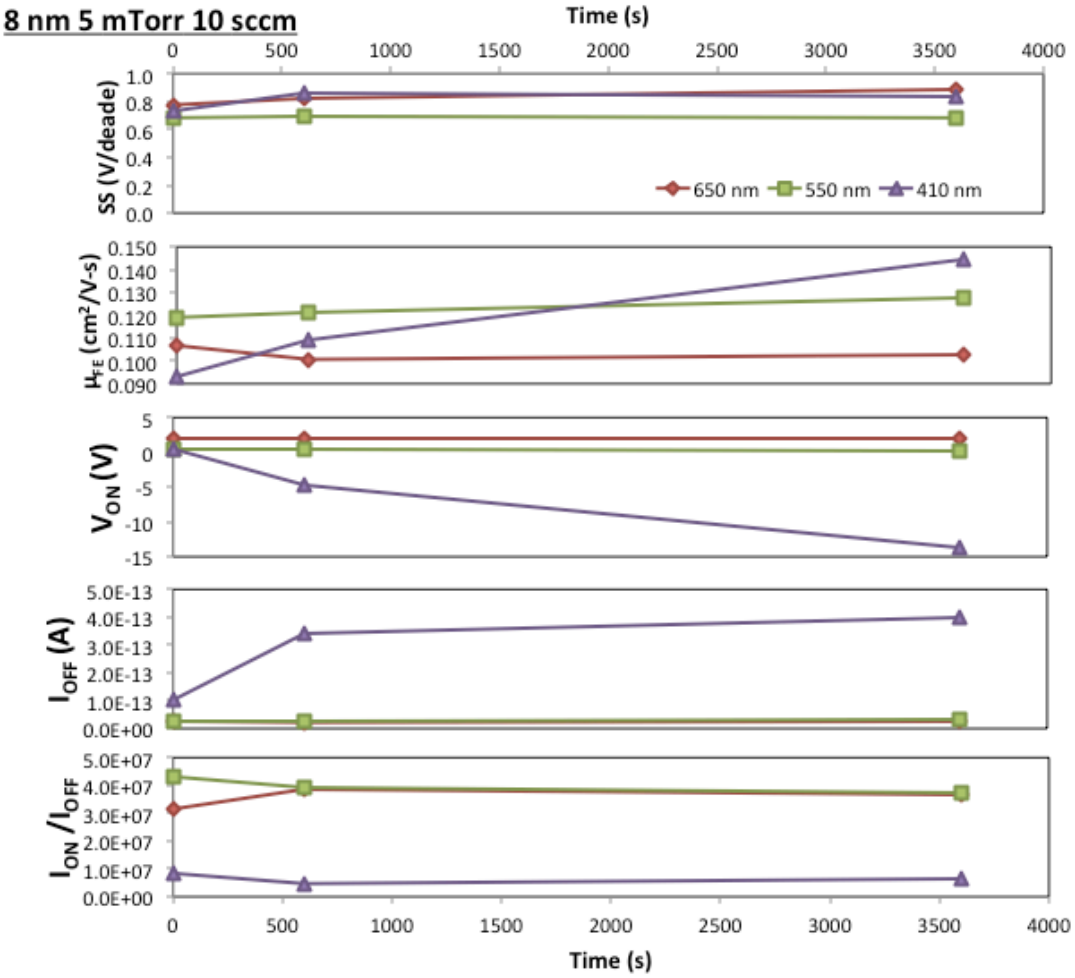

Figure A.4 High Temperature Deposition Devices

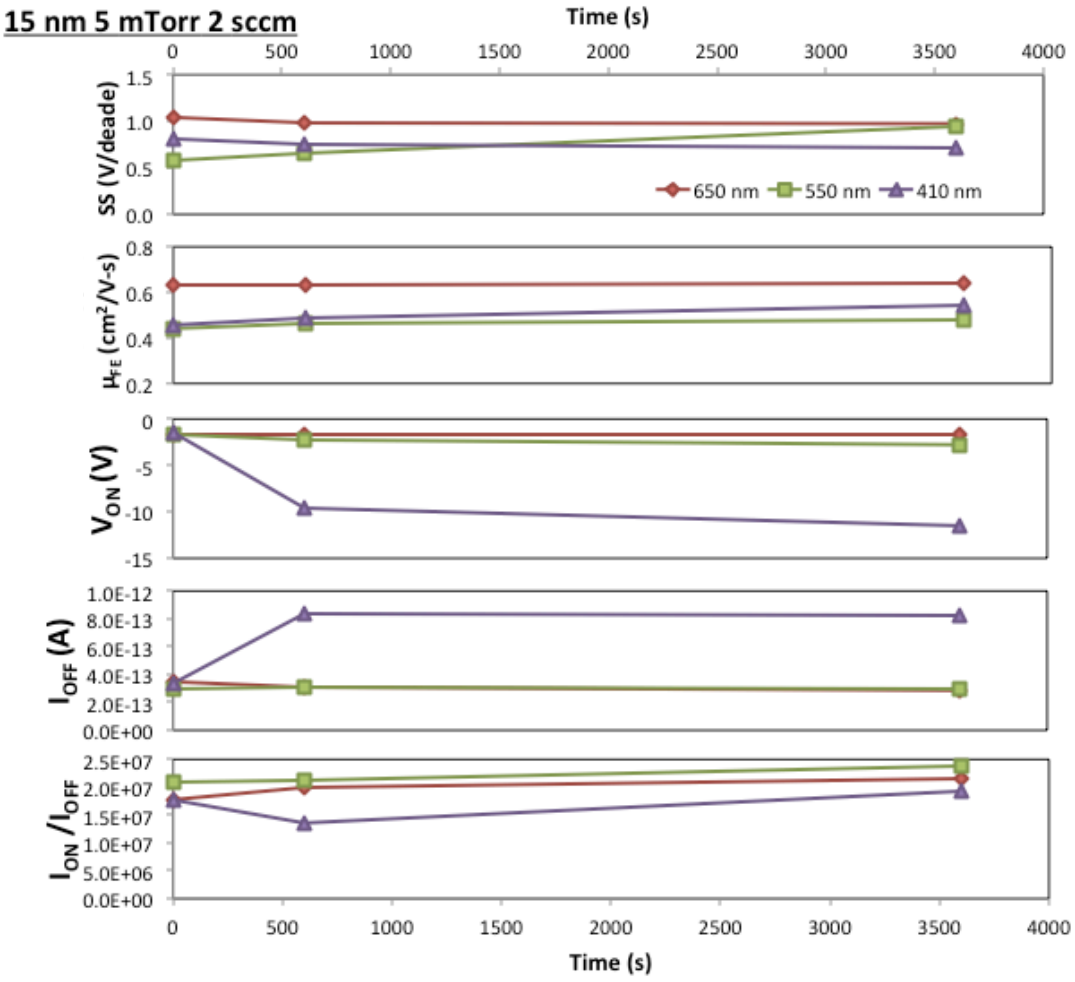

Figure A.5 High Temperature Deposition Devices

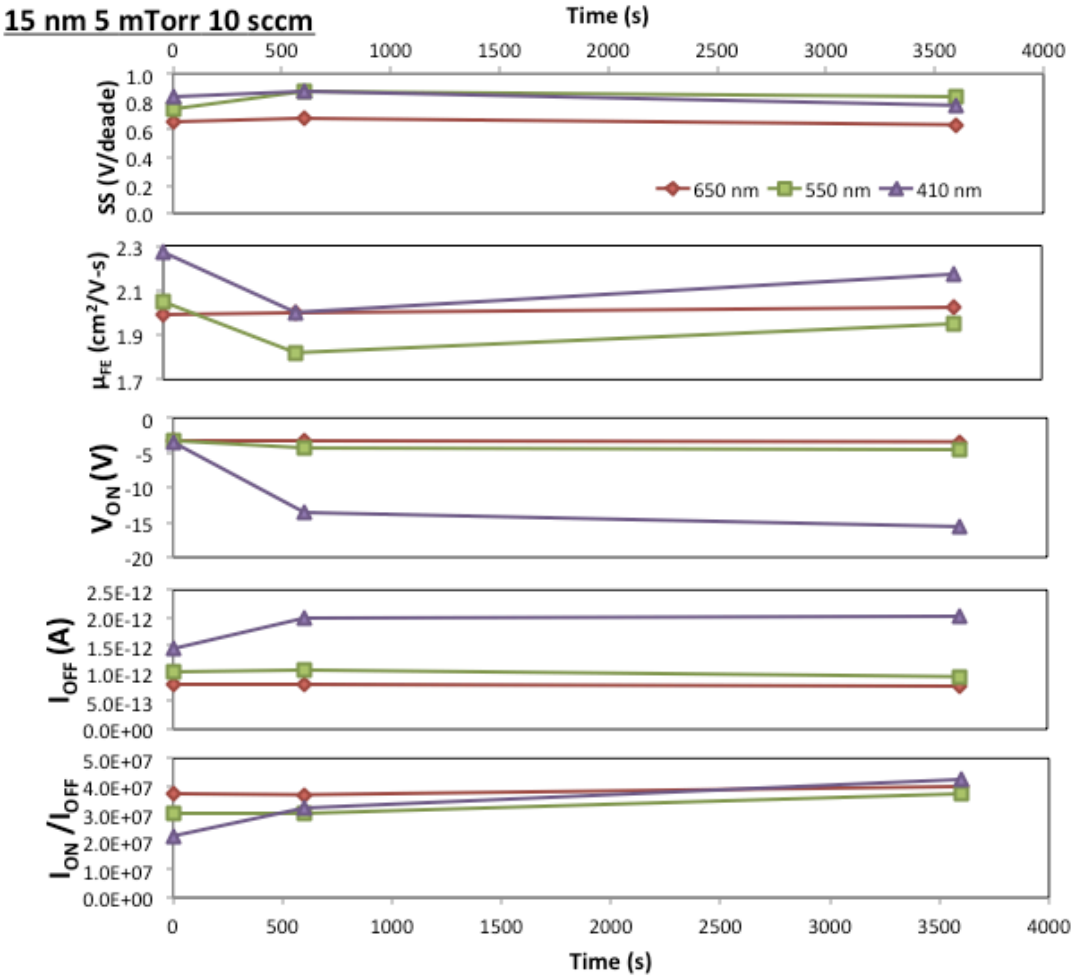

Figure A.6 High Temperature Deposition Devices

Presentations

McCall, B., Nguyen, N., Alston, R., and Li, Ji., & Iyer. S. A Comparison of the Stability of Low and High Temperatures GSZO TFTs. Annual Graduate Student Poster Competition. North Carolina Agricultural and Technical State University. April 2014

McCall, B., Nguyen, N., Alston, R., and Li, Ji., & Iyer. S. Improved Characteristics & Bias Stress Stability of GSZO Thin Film Transistors on Annealing. Poster Sessions at NAS Committee on Review of ARL Programs for HBCU/MI, North Carolina Agricultural and Technical State University. February 2014.

McCall, B., Nguyen, N., Alston, R., and Li, Ji., & Iyer. Improved Characteristics & Bias Stress Stability of GSZO Thin Film Transistors on Annealing. 2013 MRS/ASM/AVS/AReMS Joint Symposium at North Carolina State University. November 2013.

McCall, B., Nguyen, N., Alston, R., and Li, Ji., & Iyer. Improved Characteristics & Bias Stress Stability of GSZO Thin Film Transistors on Annealing. Poster Session at the NanoManufacturing 2013 Conference, Joint School of Nanoscience and Nanoengineering. September 2013.